\[ V_o = \begin{cases} 
V_{cc} & \text{cutoff} \\
V_{cc} - \beta_F (V_i - V_T) \frac{R_c}{R_B} & \text{linear} \\
V_{CE} (sat) & \text{saturation} 
\end{cases} \]

If \( V_i(t) \) is a TTL signal, then \( V_o(t) \) is also and the complement of \( V_i(t) \).
Low Noise Margin $NM_L = V_{IL} - V_{OL}$

High Noise Margin $NM_H = V_{OH} - V_{IH}$
Figure 8-10  7404 TTL INVERTER.

Standard TTL

Inverter
Standard TTL NAND gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
</tbody>
</table>
Schatthy
Diode

Schatthy
Transistor

\[ V^+ = V_{CC} = 5V \]

\[ R_{B1} = 20k \Omega \]
\[ R_{C1} = 8k \Omega \]
\[ R_{C3} = 120 \Omega \]
\[ R_{E1} = 1.5k \Omega \]
\[ R_{E2} = 4k \Omega \]
\[ R_{C3} = 3k \Omega \]

Ty L500 NAND Gate
CMOS INVERTER

For N-channel Enhancement Mode MOSFET if $V_{GS} > V_{TO}$, D to S is a short, below open.

For P-channel Enhancement Mode MOSFET if $V_{SG} > |V_{TO}|$, D to S is a short, below open.

or $|V_{GS}| > |V_{TO}|$

D to S is a short.
CMOS NOR  

\[ \begin{array}{ccc} 
A & B & Y \\
L & L & H \\
L & H & L \\
H & L & L \\
H & H & L \\
\end{array} \]  

CMOS NAND  

\[ \begin{array}{ccc} 
A & B & Y \\
L & L & H \\
L & H & H \\
H & L & L \\
H & H & L \\
\end{array} \]
**Propagation Delay**

\[ V_i \rightarrow \text{Inverter} \rightarrow V_o \]

\[ V_i(t) \]

\[ V_o(t) \]

\[ t_p = \frac{t_{PLH} + t_{PHL}}{2} \equiv \text{Propagation Delay} \]
Ring Oscillator

Inverter

\[ V_o(t) \]

\[ V_o(t) \]

\[ t_{PLH}, t_{PHL} \]

\[ T = t_{PLH} + t_{PHL} = 2T_P \]

\[ f_o = \frac{1}{T} = \frac{1}{2T_P} \]

If \( N \) inverters are cascaded

\[ T = N(t_{PLH} + t_{PHL}) \]

\[ T_P = \frac{1}{2N f_o} \quad N \text{ has to be odd} \]
Georgia Institute of Technology
School of Electrical and Computer Engineering

ECE 3042 Microelectronic Circuits Laboratory Verification Sheet

NAME: ___________________________  SECTION: _______________________
GT NUMBER: _____________________  GTID: _______________________

Experiment 8: Digital Electronic Circuits

<table>
<thead>
<tr>
<th>Procedure</th>
<th>Time Completed</th>
<th>Date Completed</th>
<th>Verification (Must demonstrate circuit)</th>
<th>Points Possible</th>
<th>Points Received</th>
</tr>
</thead>
<tbody>
<tr>
<td>2. BJT Inverter</td>
<td></td>
<td></td>
<td></td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>3. Standard TTL Inverter</td>
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<td>25</td>
<td></td>
</tr>
<tr>
<td>4. 74LS TTL Inverter</td>
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<td>25</td>
<td></td>
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<tr>
<td>5. CMOS Inverter</td>
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<td></td>
<td>25</td>
<td></td>
</tr>
</tbody>
</table>

To be permitted to complete the experiment during the open lab hours, you must complete at least three procedures during your scheduled lab period or spend your entire scheduled lab session attempting to do so. A signature below by your lab instructor, Dr. Brewer, or Dr. Robinson permits you to attend the open lab hours to complete the experiment and receive full credit on the report. Without this signature, you may use the open lab to perform the experiment at a 50% penalty.

SIGNATURE: ___________________________  DATE: ___________________________
ECE 3042 Check-off Requirements for Experiment 8

Make sure you have made all required measurements before requesting a check-off. For all check-offs, you must demonstrate the circuit or measurement to a lab instructor. All screen captures must have a time/date stamp.

2. BJT Inverter
   ✓ Screen capture of output voltage versus input voltage for $Z_L = \infty$. Adjust x & y scales so that plot uses most of the scope screen.
   ✓ Measurement of $\text{VIL, VIH, VOL, VOH, NML, }$ and $\text{NMH with scope cursors. Reference Fig. 8.7 and Eqns. 8.1 & 8.2.}$
   ✓ Screen capture of 100kHz 5 Vpp 2.5V dc square wave input and output voltage for $Z_L = \infty$. Measurement of rise time, fall time, and storage time with scope cursors.
   ✓ Screen capture of 100kHz 5 Vpp 2.5V dc square wave input and output voltage for $Z_L = \infty$ and 300pF cap across $R_b$. Measurement of rise time, fall time, and storage time with scope cursors.
   ✓ Screen capture of 100kHz 5 Vpp 2.5V dc square wave input and output voltage for $Z_L = \infty$ and diode from base to collector. Measurement of rise time, fall time, and storage time with scope cursors.

3. Standard TTL Inverter
   ✓ Screen capture of output voltage versus input voltage for $Z_L = \infty$. Adjust x & y scales so that plot uses most of the scope screen.
   ✓ Measurement of $\text{VIL, VIH, VOL, VOH, NML, }$ and $\text{NMH with scope cursors. Reference Fig. 8.7 and Eqns. 8.1 & 8.2.}$
   ✓ Screen capture of 100kHz 5 Vpp 2.5V dc square wave input and output voltage for $Z_L = \infty$.
   ✓ Screen capture of 100kHz 5 Vpp 2.5V dc square wave input and output voltage at collector of Q3.
   ✓ Previous two requirements repeated for $f$ changed to 1MHz.

4. 74LS TTL Inverter
   ✓ Screen capture of output voltage versus input voltage for $Z_L = \infty$. Adjust x & y scales so that plot uses most of the scope screen.
   ✓ Measurement of $\text{VIL, VIH, VOL, VOH, NML, }$ and $\text{NMH with scope cursors. Reference Fig. 8.7 and Eqns. 8.1 & 8.2.}$
   ✓ Screen capture of 100kHz 5 Vpp 2.5V dc square wave input and output voltage for $Z_L = \infty$.
   ✓ Screen capture of 1MHz 5 Vpp 2.5V dc square wave input and output voltage for $Z_L = \infty$.
   ✓ Measurement of average power dissipation per gate for no input, 100kHz 5 Vpp 2.5V dc square wave input, and 1MHz 5 Vpp 2.5V dc square wave input.

5. CMOS Inverter
   ✓ Screen capture of output voltage versus input voltage for $Z_L = \infty$. Adjust x & y scales so that plot uses most of the scope screen.
   ✓ Measurement of $\text{VIL, VIH, VOL, VOH, NML, }$ and $\text{NMH with scope cursors. Reference Fig. 8.7 and Eqns. 8.1 & 8.2.}$
   ✓ Screen capture of 100kHz 10 Vpp 5V dc square wave input and output voltage for $Z_L = \infty$.
   ✓ Screen capture of 100kHz 10 Vpp 5V dc square wave input and output voltage for 1nF load cap.
   ✓ Measurement of average power dissipation per gate for both a 100kHz 10 Vpp 5V dc square wave input and a 15MHz 10 Vpp 5V dc square wave input.