1. Design the circuit below so that the small signal input impedance is 30 k\(\Omega\), the small signal midband gain is \(-10\), dc collector current in \(Q_1\) is 1 mA, and the circuit clips symmetrically. Simulate the circuit shown below with SPICE. Use the SPICE parameters for the NPN transistor given in the Preliminary SPICE Simulations sections. Obtain the dc operating point, an ac analysis, and a transient analysis sufficient to show the clipping behavior. Use the component values: \(C_1 = C_2 = 22 \mu F\), \(C_E = 330 \mu F\), \(R_E = 1 k\Omega\), and \(R_L = 1 k\Omega\). Assume that the collector to emitter saturation voltage \(V_{CE(sat)} = 0.2 V\) and \(V^+ = 15 V\).