1. Shown is a two stage discrete transistor voltage amplifier. The input stage uses a N Channel JFET. The second stage is a PNP BJT. JFETs have large input impedances and, therefore, don’t load the input voltage source as much as other devices. They also have the least noise of any semiconductor device. The parameters of the JFET are: 
\[ I_{DSS} = 10 \text{mA}, \ V_T = -3 \text{V}, \ \text{and} \ \lambda = 0.001 \text{V}^{-1}. \] 
Bias the circuit so that \( I_D = I_{DSS}/2 \) and \( V_C = 5 \text{V} \). Assume that \( R_C = 1 \text{k}\Omega \) and for design calculation purposes and the \( \beta \) of the BJT is \( \infty \). Pick \( R_F = 2R_S, R_L = 30 \text{k}\Omega, \) and \( R_G = 10 \text{M}\Omega \). (Hint: Once the drain current is specified this sets the gate-to-source voltage. The gate voltage is zero since the input impedance of the JFET is \( \infty \) at dc. So the source voltage is set. Then compute the other resistors.)

2. Use Multisim to perform a dc operating point (the current in both transistors), Bode plot (1 Hz to 100 MHz), the clipping behavior, and a noise analysis over the same frequency range as the Bode plot. (Noise is an undesired signal which much be described using probability. Physical sources are thermal noise, shot noise, and \( 1/f \) noise. It differs from power line ripple and interference. Plot the output noise spectrum with the input voltage as the reference.) Use the device model in the Multisim parts library for the PNP BJT (use 2N3906).

3. This circuit uses feedback from the output node to the input node. (Feedback is a topic which will be extensively used in Exp 8.) The type of feedback is series-shunt. For this type of amplifier the voltage gain is given by
\[
A_v = \frac{A}{1+Ab}
\]
where \( A_v \) is the voltage gain, \( A \) is the open loop gain of the circuit, and \( b \) is the feedback factor given by
\[
b = \frac{R_S}{R_S + R_F}
\]
Determine from the SPICE simulation what the midband voltage gain is, \( A_v \), and compute the value of the open loop gain \( A \). Place a 10 \( \mu \text{F} \) capacitor from the emitter to ground and repeat the AC analysis and recompute the open loop gain.