1. Design the Common Source JFET amplifier shown below. Bias it at a current of $I_D = I_{DSS}/2$, $V_D = V^+/2$, and $V_S = V^-/2$. Use the parameters $\beta = 1.35 \text{ mA/V}^2$, $V_{TO} = -1.8 \text{ V}$, $R_d = 35 \Omega$, $R_s = 31.5 \Omega$, $K_f = 6.5 \times 10^{-17}$, $A_f = 0.5$, $C_{gs} = 2.25 \text{ pF}$, $C_{gd} = 6 \text{ pF}$, and $\lambda = 0.001 \text{ V}^{-1}$. Use $C_1 = 10 \mu\text{F}$, $C_2 = 22 \mu\text{F}$, and $C_S = 100 \mu\text{F}$. The dc power supplies are $V^+ = -V^- = 15 \text{ V}$. The load resistor $R_L = 20 \text{k}\Omega$ and the small signal midband input impedance is $80 \text{k}\Omega$. The magnitude of the small signal midband voltage gain is 5.

2. Perform a SPICE simulation of the Common Source Amplifier to obtain the dc operating point, the frequency response (AC analysis), the Clipping behavior, and a noise analysis. Compare with the design specifications.