1. Shown below is a common emitter amplifier cascaded with a push pull circuit. Design the circuit below so that the small signal input impedance is 73 kΩ, the small signal midband gain is $-7.3$, and the circuit clips symmetrically. Simulate the circuit shown below with SPICE. Obtain the dc operating point, an ac analysis, and a transient analysis sufficient to show the clipping behavior. (For the ac analysis use the output as the base of $Q_2$ and $Q_3$.) Use the component values: $C_1 = C_2 = 22 \mu F$, $C_E = 330 \mu F$, $R_1 = R_2 = 100 \Omega$, $R_C = 7.3 \text{k}\Omega$, and $R_L = 1 \text{k}\Omega$. Assume that the collector to emitter saturation voltage $V_{CE(sat)} = 0.2 \text{V}$ and $V^+ = 15 \text{V} = -V^-$. For the design assume that $\beta = \infty$, $V_A = \infty$, and $V_{BE} = 0.65 \text{V}$ for the NPN transistors and that $V_{EB} = 0.65 \text{V}$ for the PNP transistor. For the simulation assume that $\beta = 100$, $V_A = 170$, and $I_{SO}$ is the value that will make the magnitude of the base to emitter voltage 0.65 V when the magnitude of the collector current is 1 mA. Repeat the transient analysis for $R_L = 10 \text{k}\Omega$. 

![Circuit Diagram](image-url)