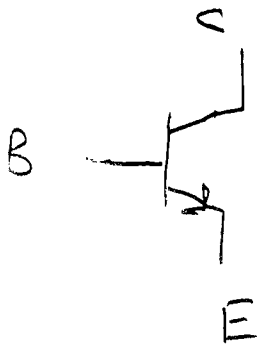
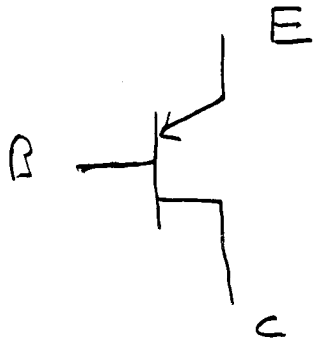
Bipolar Junction



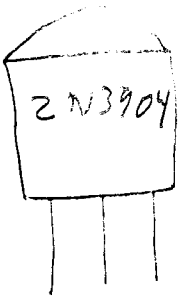
NPN



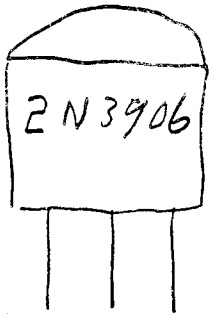
PNP

2N3904

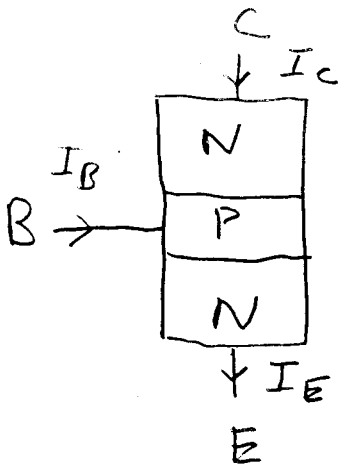
2N3906

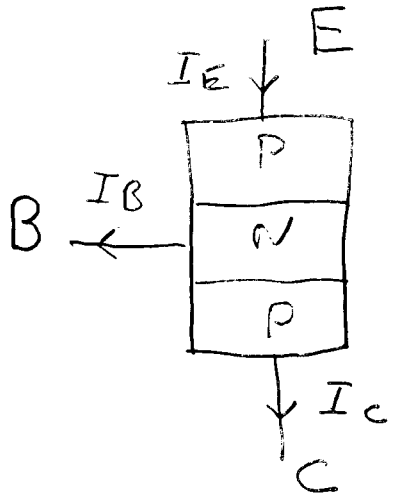


E B C



E B C





Forward Active Mode

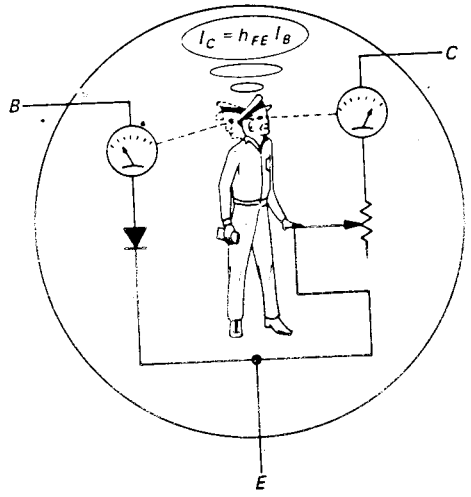
Base - Emitter Junction, Forward Biased

Collector - Base Junction, Reverse Biased

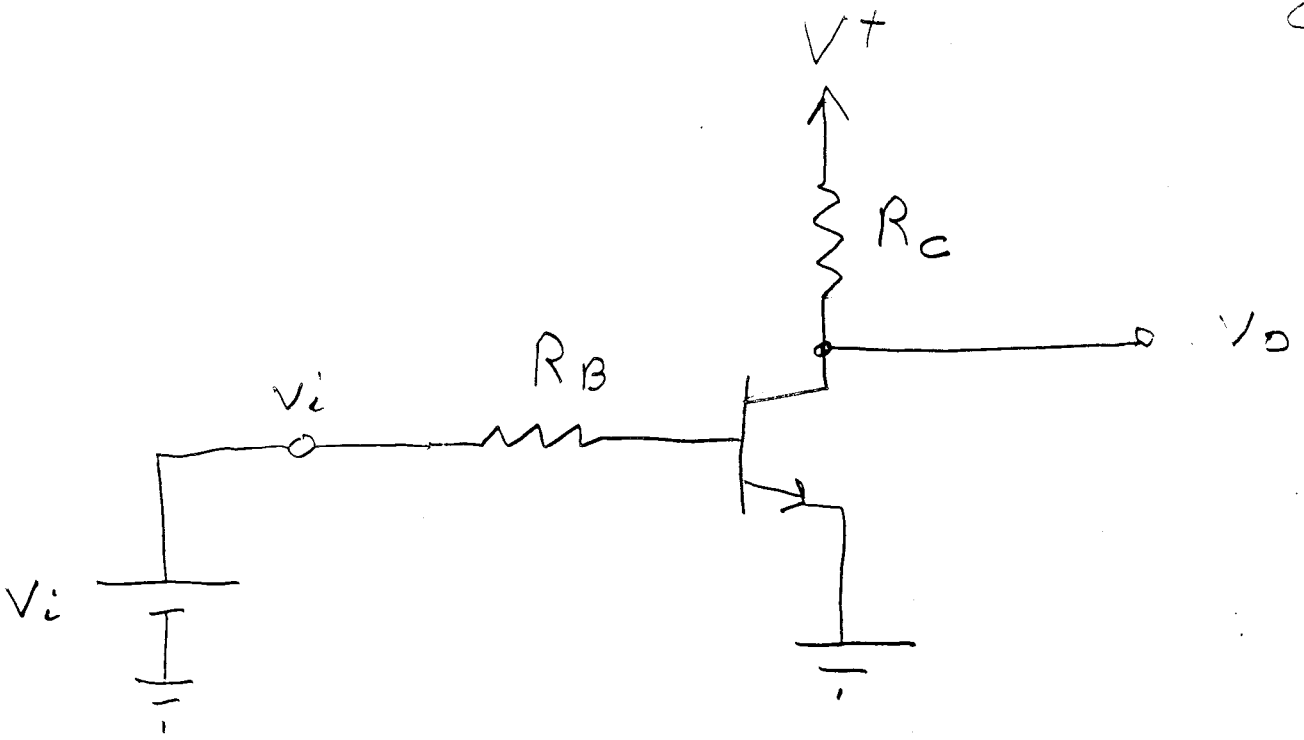
$$\beta = \frac{I_C}{I_B} = h_{FE}$$ huge

$$\alpha = \frac{I_C}{I_E}$$ < 1 & close to 1

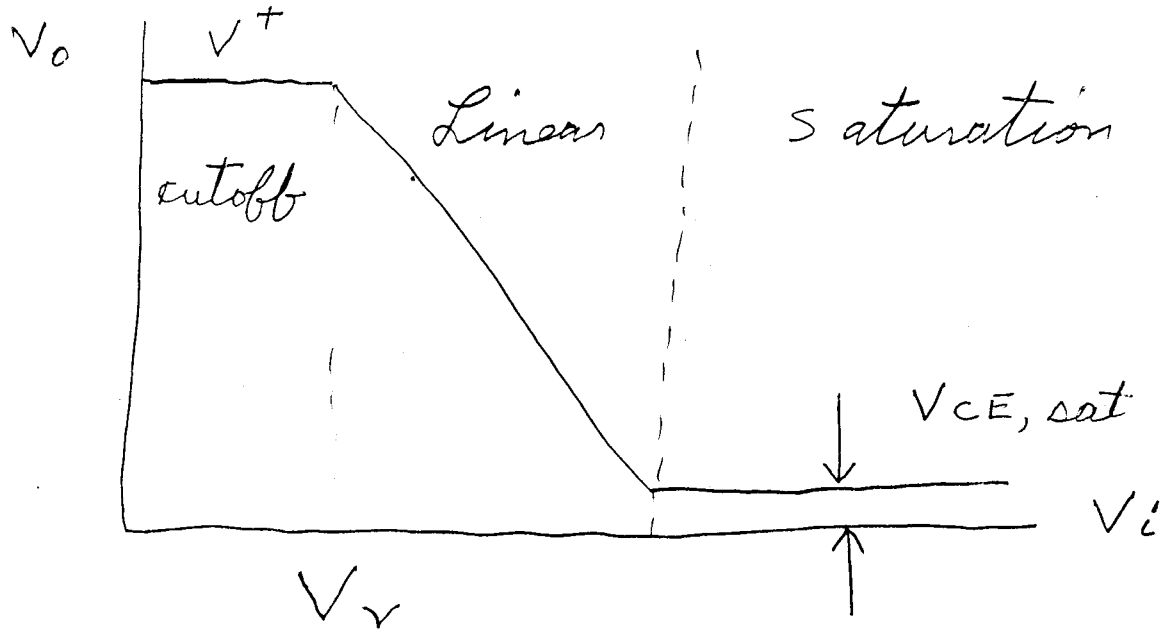
$V_{BE} \approx 0.65\ V$



Transistor Man



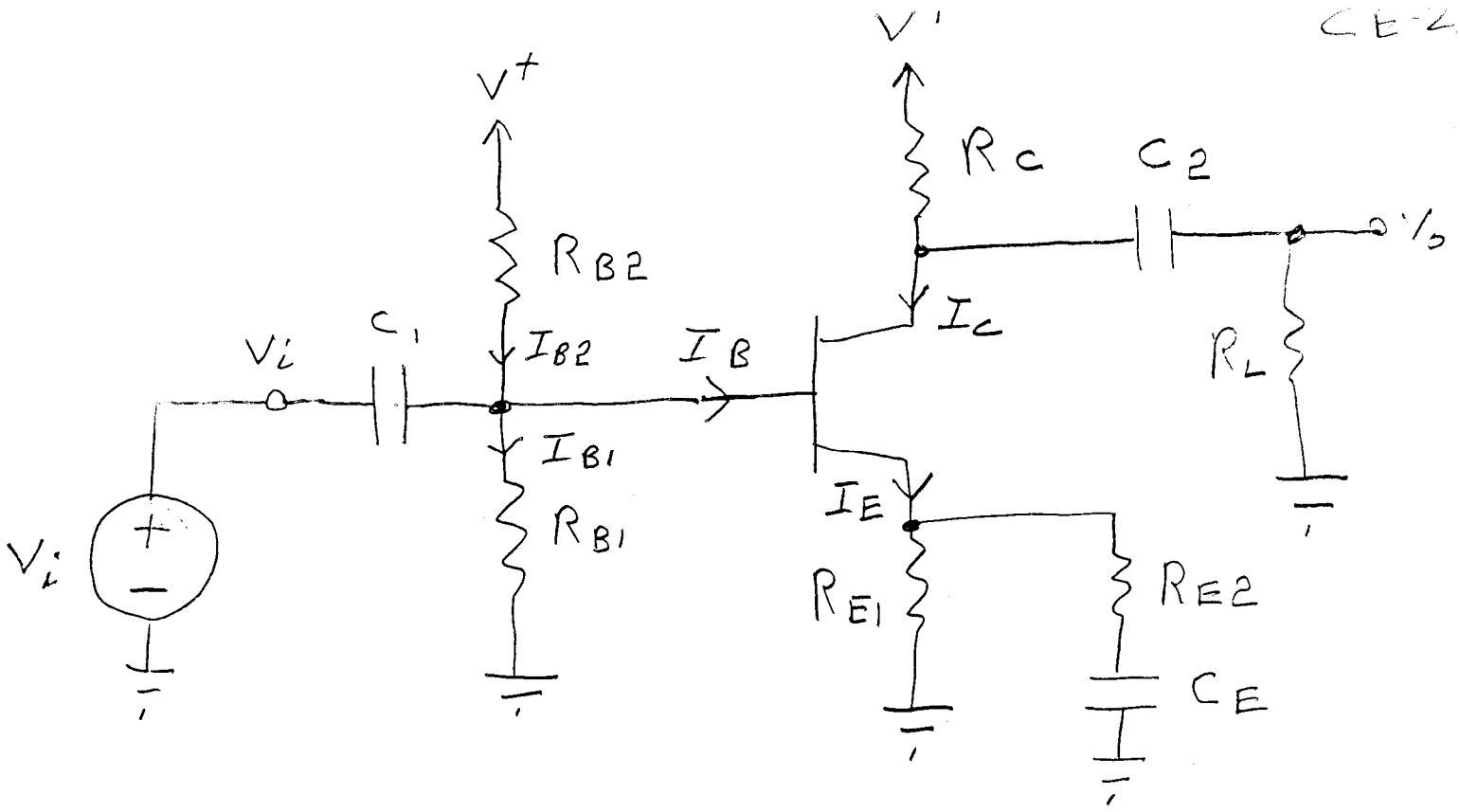
VTC – Voltage Transfer Characteristic



$V_\gamma = V_{BE} \simeq 0.65\,V$

In linear region

$$V_o = V^+ - \beta \frac{R_c}{R_B}(V_i - V_\gamma)$$



Common Emitter Amplifier

For design calculations assume $V_A = \infty$

$$A_v = -\frac{\alpha R_{tc}}{r_{ie} + R_{te}}$$

$$R_{tc} = R_c \parallel R_L \quad , \quad R_{te} = R_{E1} \parallel R_{E2}$$

$$r_{ie} = \frac{R_{tb} + r_x}{1+\beta} + r_e \quad , \quad r_e = \frac{V_T}{I_E}$$

r_e: intrinsic emitter resistance

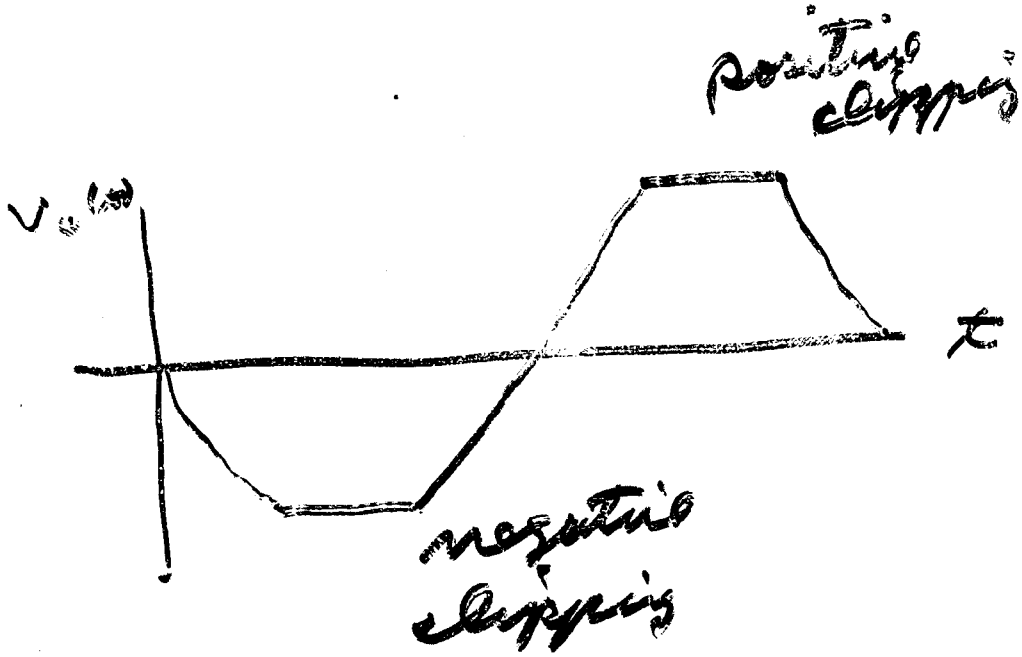
$$|A_v| \approx \alpha \frac{R_{tc}}{R_{te}} = \alpha \frac{R_c \parallel R_L}{R_{E1} \parallel R_{E2}}$$

For symmetric clipping must choose

$$I_C = \frac{V^+}{R_C \| R_L + R_C + R_{E1} + R_{E1} \| R_{E2}}$$

$$I_C = \alpha I_E$$

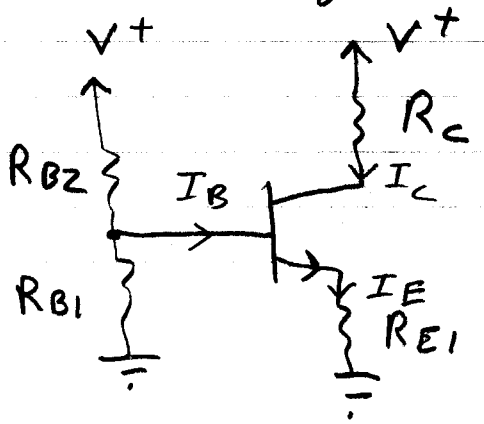
$$\alpha = \frac{\beta}{\beta + 1}$$



Common Emitter Amplifier

dc Analysis

Given R_2 & transistor parameters, find dc voltages & currents

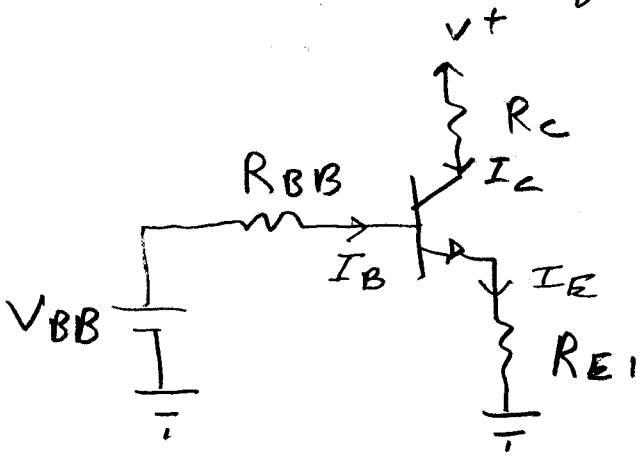


$$\beta = \frac{I_C}{I_B}$$

$$\alpha = \frac{I_C}{I_E}$$

$$\alpha = \frac{\beta}{\beta+1}$$

Find Thévenin Eq looking out of base



$$R_{BB} = R_{B1} \,||\, R_{B2}$$

$$V_{BB} = V^+ \frac{R_{B1}}{R_{B1}+R_{B2}}$$

If the transistor is in the linear region

$$V_{BB} = I_B R_{BB} + V_{BE} + I_E R_{E1}$$

cutoff $V_{BB} < V_\gamma = 0.65$ V_{BE} on voltage

$I_C = I_E = I_B = 0$

$V_E = 0$ $V_B = V_{BB}$ $V_C = V^+$

Saturation $V_{CE} = V_{CE\,sat} \simeq 0.2\,V$

$$V^+ \simeq I_C R_C + V_{CE\,sat} + I_E R_{E1}$$

$$I_C = \frac{V^+ - V_{CE\,sat}}{R_C + \frac{R_{E1}}{\alpha}}$$

This occurs for

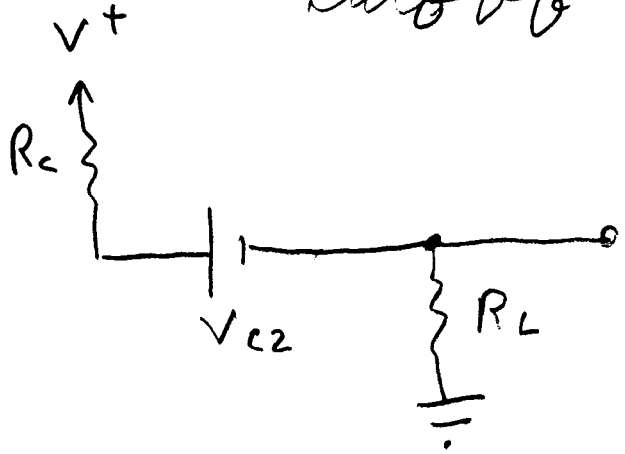
$$V_{BB} > R_{BB} I_B + V_\gamma + I_E R_{E1}$$

Clipping

The output levels at which the circuit clips are functions of R_C, R_L, R_{E1}, R_{E2}, I_C, & the transistor parameters.

The capacitors are modeled as dc batteries with values equal to the dc voltage drop across them

Cutoff

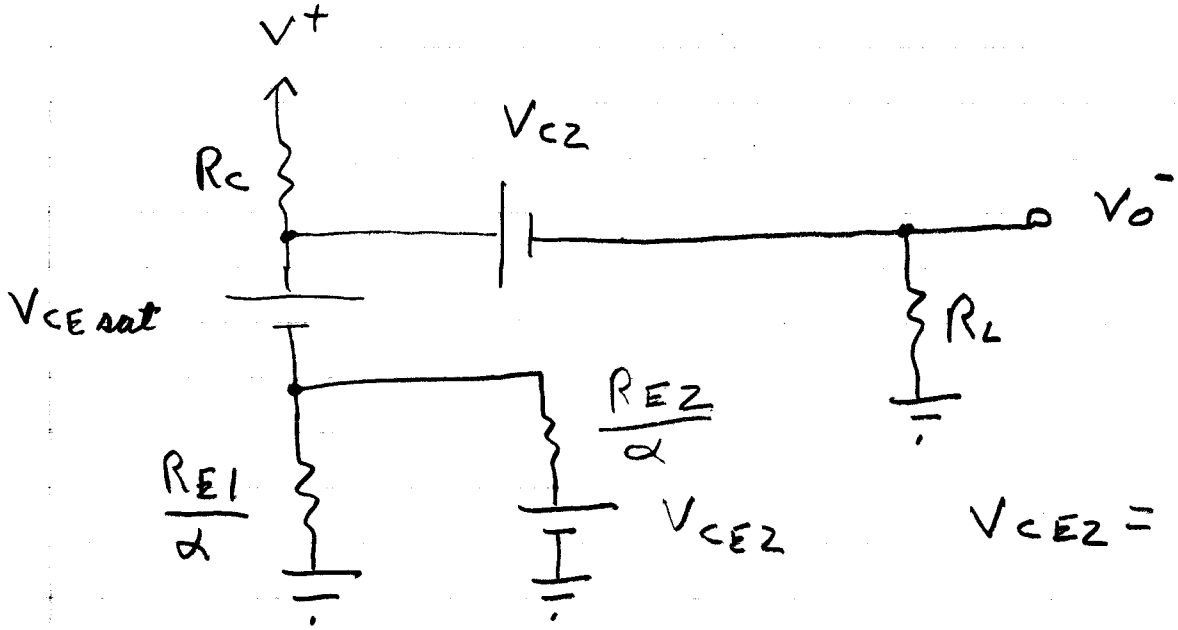


$$V_{c2} = V^+ - I_C R_C$$

$$V_o^+ = \left[V^+ - V_{c2}\right] \frac{R_L}{R_L + R_C}$$

$$V_o^+ = I_C R_C \| R_L$$

Saturation



$$V_{CE2} = I_E R_{E1}$$

$$V_o^- = -\left[V^+ - V_{CE\,sat} - I_c\left(R_c + \frac{R_{E1}}{\alpha} \right) * \frac{R_c \| R_L}{R_c \| R_L + \frac{R_{E1} \| R_{E2}}{\alpha}} \right]$$

To get symmetric clipping

set $V_o^+ = -V_o^- \Rightarrow$

$$I_c = \frac{V^+ - V_{CE\,sat}}{R_c \| R_L + R_c + \frac{R_{E1} + R_{E1} \| R_{E2}}{\alpha}}$$

Georgia Institute of Technology

School of Electrical and Computer Engineering

ECE 3042 Microelectronic Circuits Laboratory Verification Sheet

NAME:_____ SECTION:_____

GT NUMBER:_____ GTID:_____

Experiment 1: Single Stage Amplifier

Procedure	Time Completed	Date Completed	Verification (Must demonstrate circuit)	Points Possible	Points Received
1. Breadboard Prep				20	
4. Bias				20	
5,6. Small Signal Gain and Freq Response				20	
7. Clipping				20	
8. Spectral Analysis				20	

To be permitted to complete the experiment during the open lab hours, you must complete at least **four** procedures during your scheduled lab period or spend your entire scheduled lab session attempting to do so. A signature below by your lab instructor, Dr. Brewer, or Dr. Robinson permits you to attend the open lab hours to complete the experiment and receive full credit on the report. Without this signature, you may use the open lab to perform the experiment at a 50% penalty.

SIGNATURE:_____ DATE:_____

ECE 3042 Check-off Requirements for Experiment 1

Make sure you have made all required measurements before requesting a check-off. For all check-offs, you must demonstrate the circuit or measurement to a lab instructor. All screen captures must have a time/date stamp.

1. Breadboard Preparation
   - ✓ Power supply connected to breadboard binding posts.
   - ✓ 100 ohm resistors in series with binding posts to positive and negative rails on breadboard.
   - ✓ Wire from ground post to ground rail on board.
   - ✓ Decoupling capacitors in place and correctly oriented.

4. Bias
   - ✓ Collector, base, and emitter voltages and collector current recorded.

5, 6 . Gain and Frequency Response
   - ✓ Oscilloscope screen capture showing input and output signals and Vpp measurements for each signal.
   - ✓ Calculation of the gain.
   - ✓ Plot of gain versus frequency made with HPVEE, LabView, or by hand with -3dB frequencies and midband gain labeled and their values recorded.

7. Clipping
   - ✓ Screen capture showing soft clipping on output and measured positive and negative peak amplitudes (can use max and min functions on scope).
   - ✓ Screen capture displaying hard clipping on output and measured positive and negative clipping levels (can use max and min functions on scope).
   - ✓ Screen capture of XY plot when amplifier is clipped.
   - ✓ Calculation of slope of XY plot (use scope cursors).

8. Spectral Analysis
   - ✓ Screen capture showing fundamental and distortion components.
   - ✓ Screen capture after adjusting pot to maximize amplitude of fundamental but eliminate distortion components.
   - ✓ Measured circuit gain after pot adjustment.
   - ✓ Measured pot value (disconnect pot from circuit before measuring).