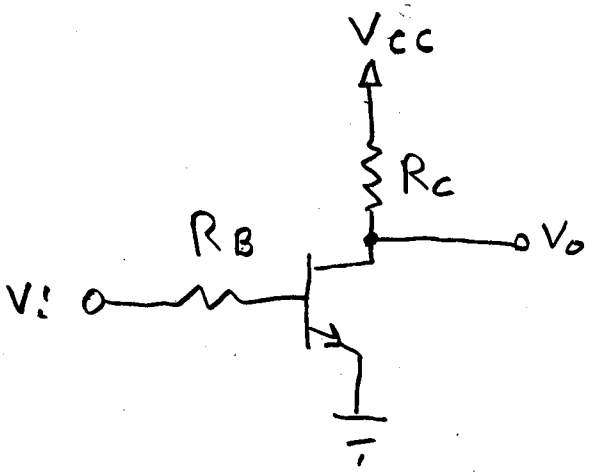
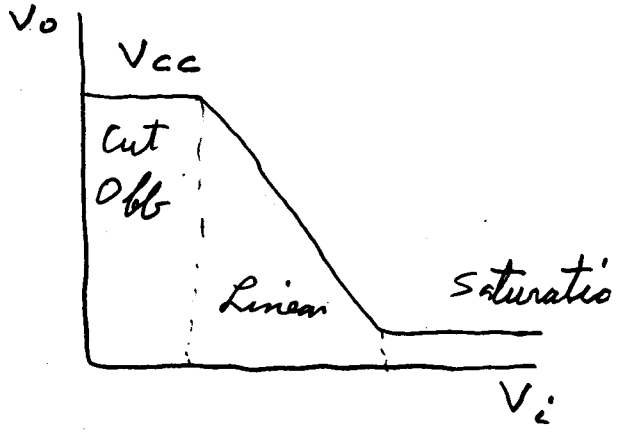
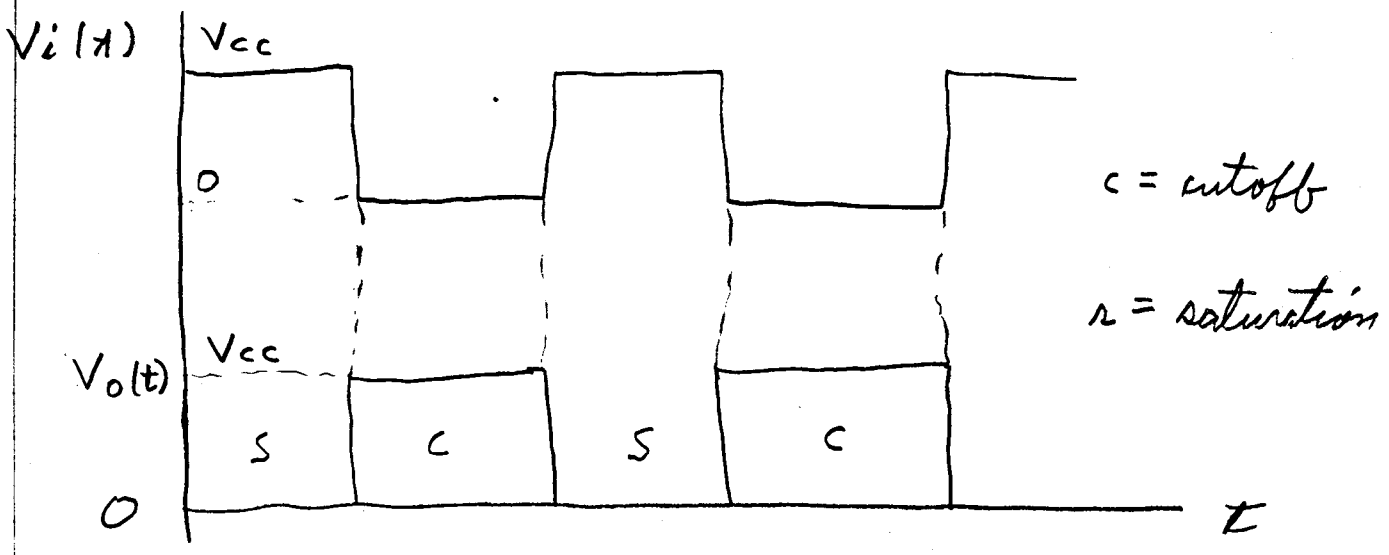
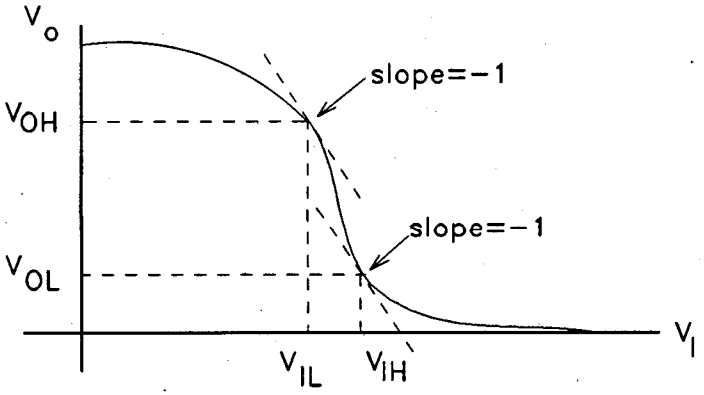




$$V_o = \begin{cases} V_{cc} & \text{cutoff} \\ V_{cc} - \beta_F (V_i - V_r) \dfrac{R_c}{R_B} & \text{linear} \\ V_{CE(sat)} & \text{saturation} \end{cases}$$

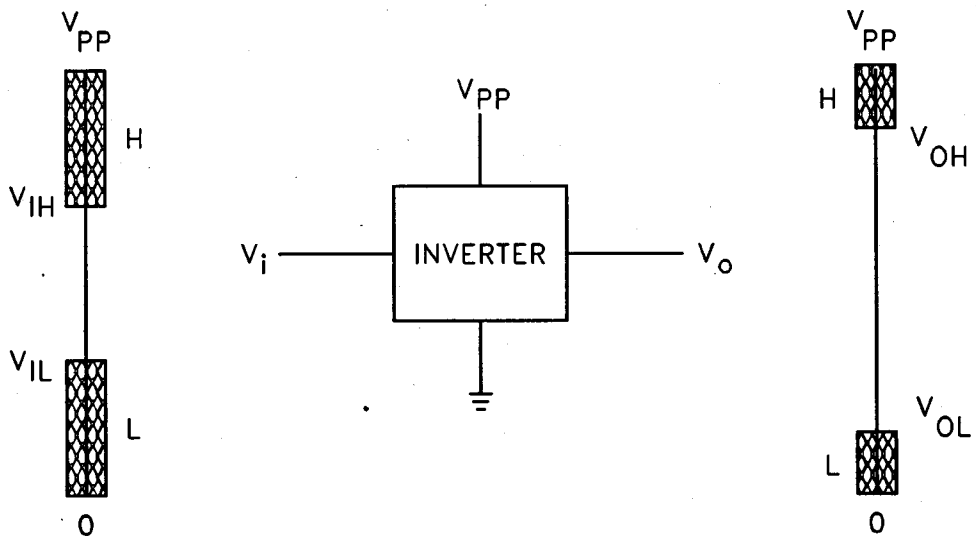
If $V_i(t)$ is a TTL signal, then $V_o(t)$ is also and the complement of $V_i(t)$





Low Noise Margin $NM_L = V_{IL} - V_{OL}$

High Noise Margin $NM_H = V_{OH} - V_{IH}$



DE-2

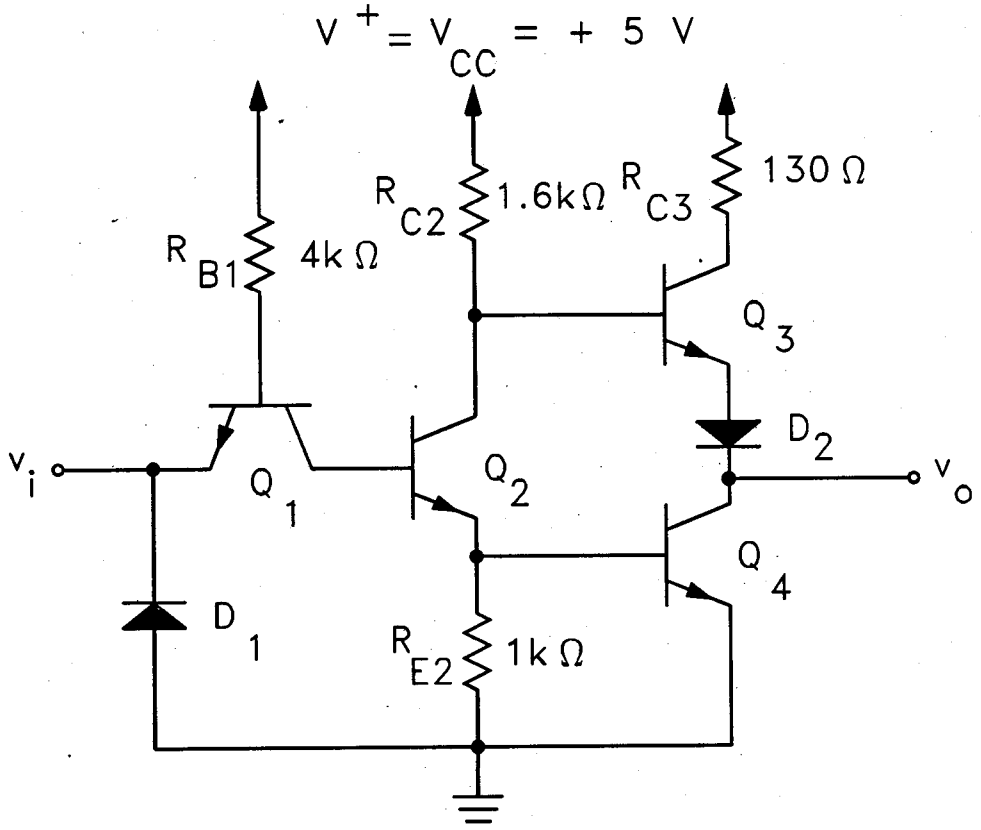
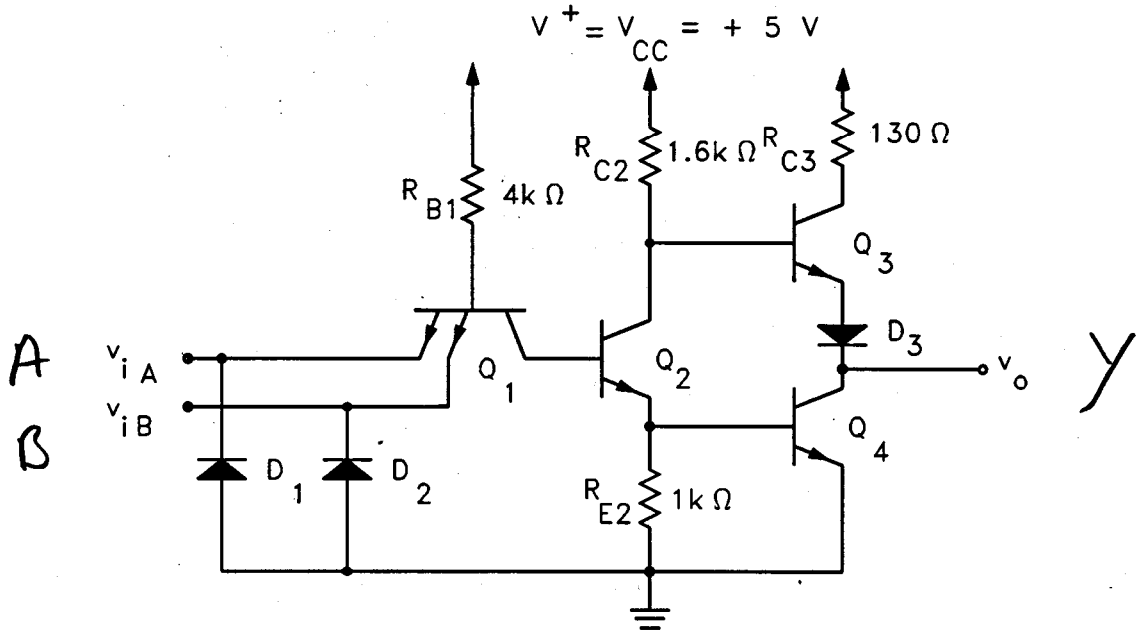


Figure 8-10 7404 TTL *INVERTER.*

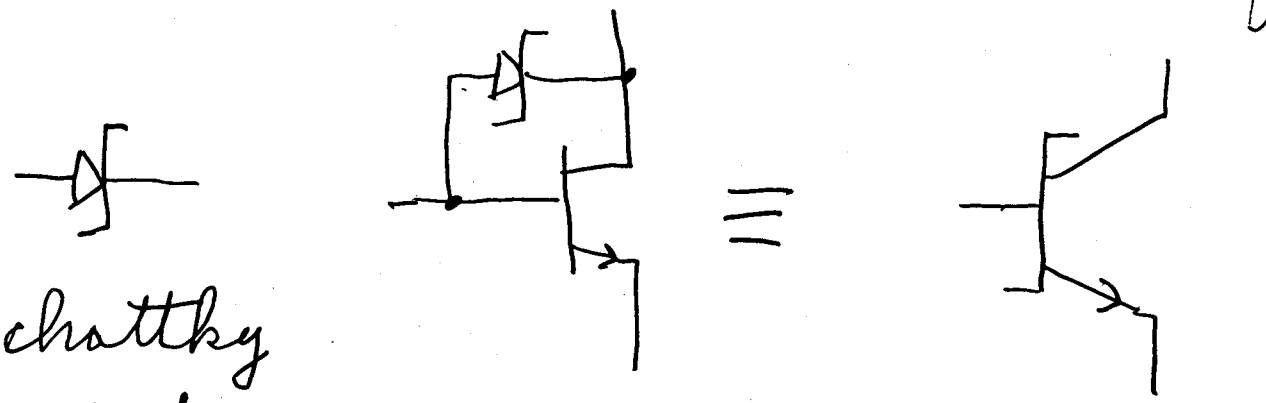
standard TTL Inverter



Standard TTL NAND Gate

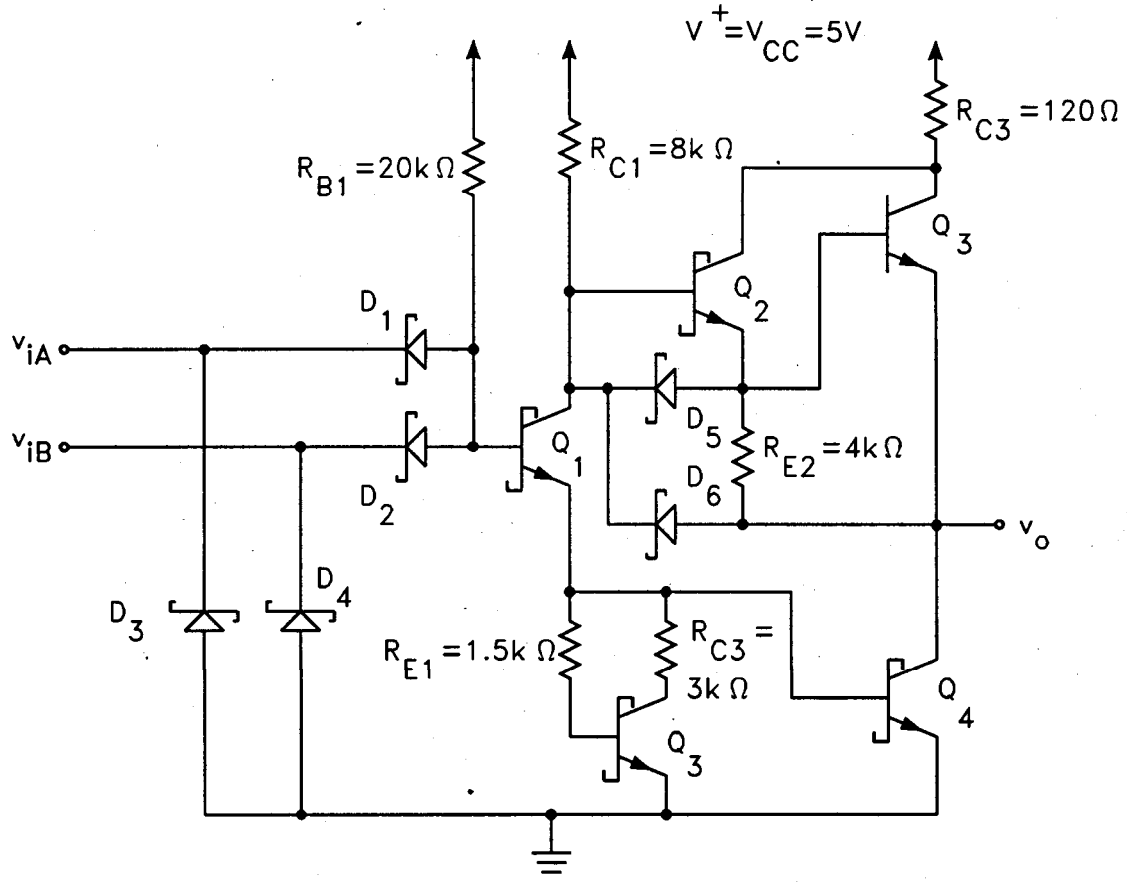
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

7400

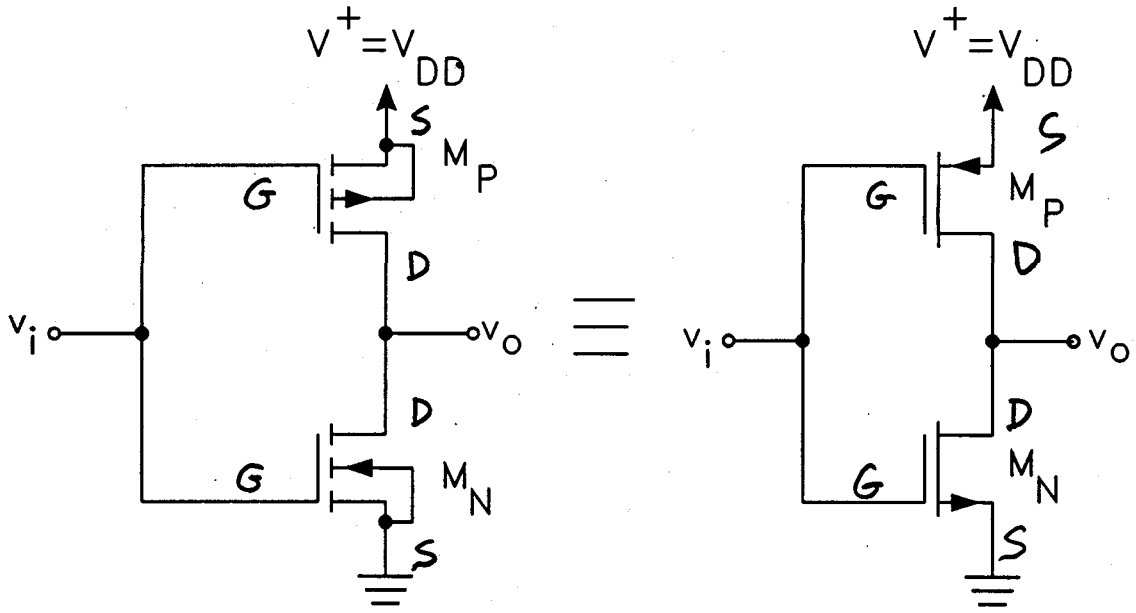


Schottky Diode

Schottky Transistor



74LS00 NAND Gate



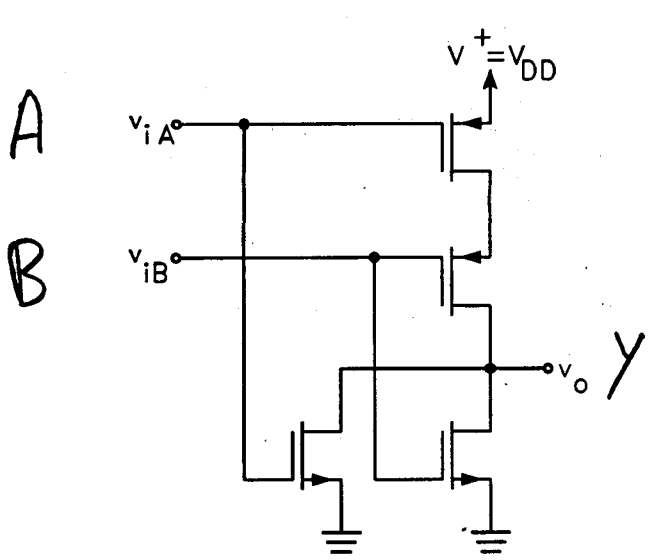
CMOS INVERTER

For N channel Enhancement Mode Mosfet if $V_{GS} > V_{TO}$ D to S is a short, below open

For P channel Enhancement Mode Mosfet if $V_{SG} > |V_{TO}|$ D to S is a short, below open

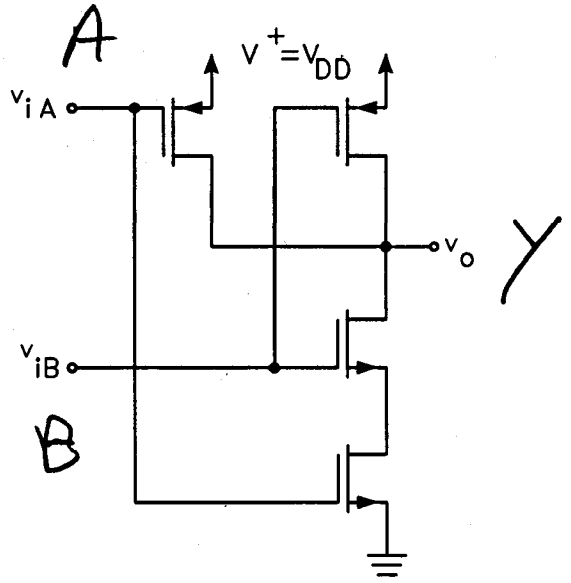
or $|V_{GS}| > |V_{TO}|$

D to S is a short



CMOS NOR

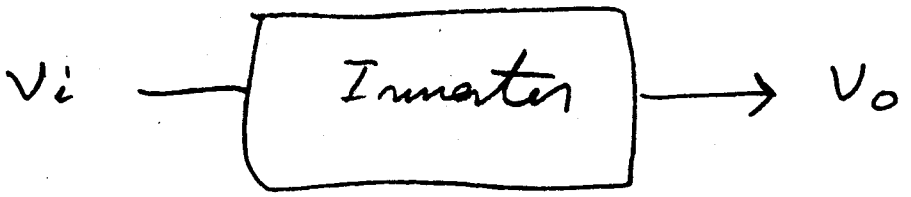
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

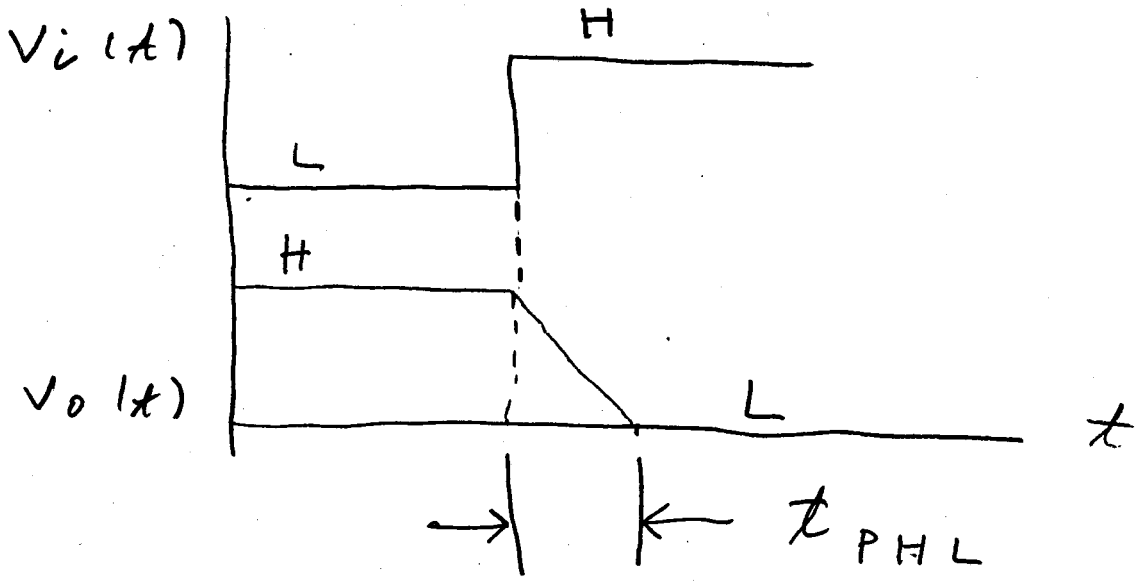


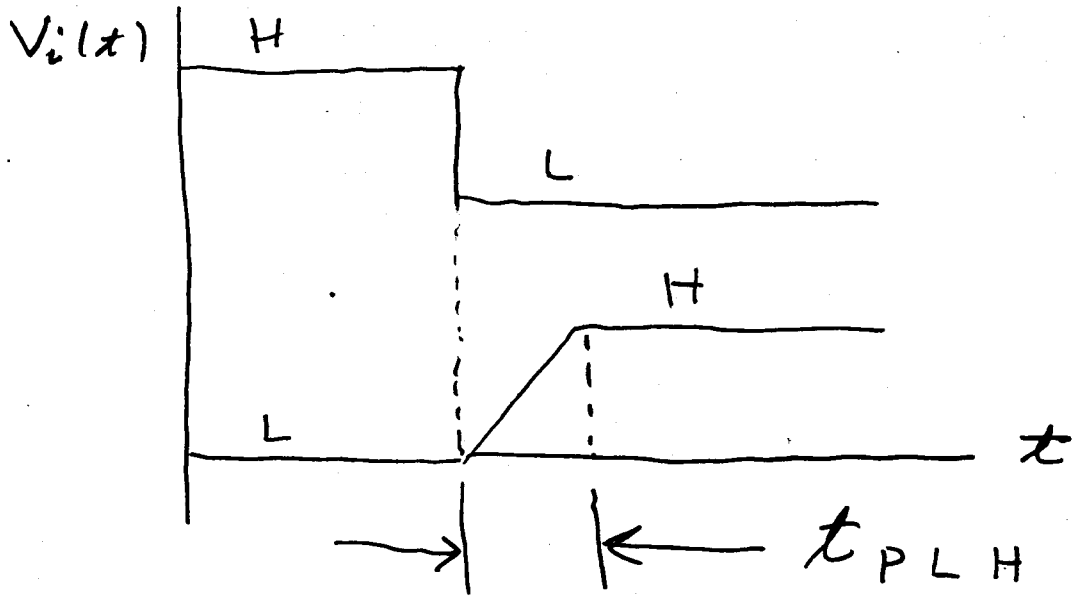
CMOS NAND

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Propagation Delay



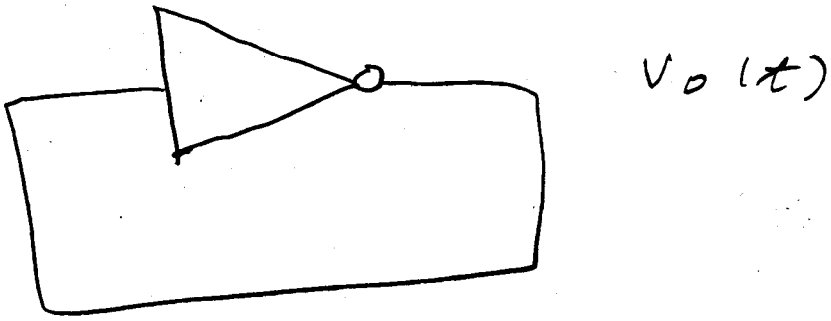


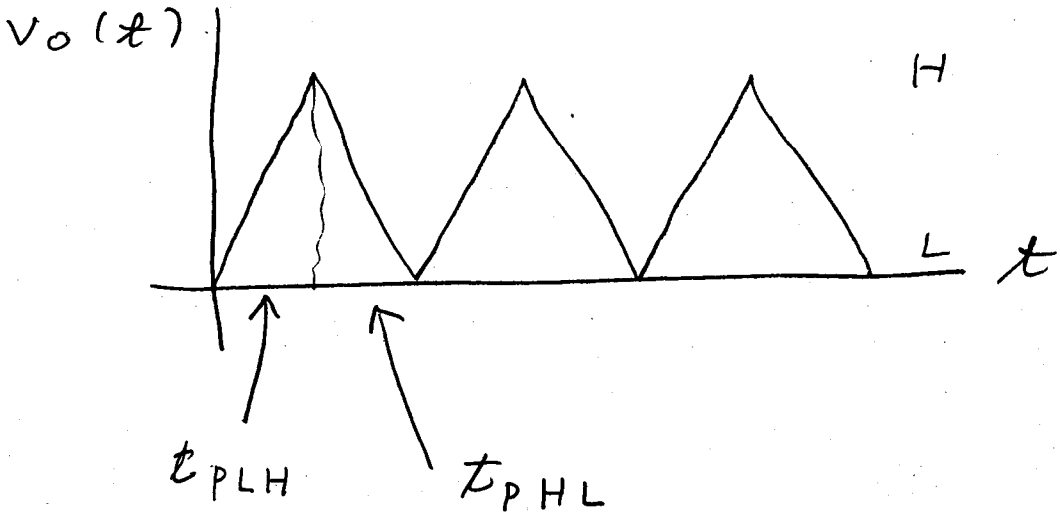


$$t_p = \frac{t_{PLH} + t_{PHL}}{2} \equiv \text{Propagation Delay}$$

Ring Oscillator

Inverter





$$T = t_{PLH} + t_{PHL} = 2t_p$$

$$f_o = \frac{1}{T} = \frac{1}{2t_p}$$

If N inverters are cascaded

$$T = N(t_{PLH} + t_{PHL})$$

$$t_p = \frac{1}{2N f_o}$$

N has to be odd

Georgia Institute of Technology

School of Electrical and Computer Engineering

ECE 3042 Microelectronic Circuits Laboratory Verification Sheet

NAME:_____ SECTION:_____

GT NUMBER:_____ GTID:_____

Experiment 8: Digital Electronic Circuits

Procedure	Time Completed	Date Completed	Verification (Must demonstrate circuit)	Points Possible	Points Received
2. BJT Inverter				25	
3. Standard TTL Inverter				25	
4. 74LS TTL Inverter				25	
5. CMOS Inverter				25	

To be permitted to complete the experiment during the open lab hours, you must complete at least **three** procedures during your scheduled lab period or spend your entire scheduled lab session attempting to do so. A signature below by your lab instructor, Dr. Brewer, or Dr. Robinson permits you to attend the open lab hours to complete the experiment and receive full credit on the report. Without this signature, you may use the open lab to perform the experiment at a 50% penalty.

SIGNATURE:_____ DATE:_____

ECE 3042 Check-off Requirements for Experiment 8

Make sure you have made all required measurements before requesting a check-off. For all check-offs, you must demonstrate the circuit or measurement to a lab instructor. All screen captures must have a time/date stamp.

2. BJT Inverter
   - ✓ Screen capture of output voltage versus input voltage for $Z_L = \infty$. Adjust x & y scales so that plot uses most of the scope screen.
   - ✓ Measurement of VIL, VIH, VOL, VOH, NML, and NMH with scope cursors. Reference Fig. 8.7 and Eqns. 8.1 & 8.2.
   - ✓ Screen capture of 100kHz 5 Vpp 2.5V dc square wave input and output voltage for $Z_L = \infty$. Measurement of rise time, fall time, and storage time with scope cursors.
   - ✓ Screen capture of 100kHz 5 Vpp 2.5V dc square wave input and output voltage for $Z_L = \infty$ and 300pF cap across R_B. Measurement of rise time, fall time, and storage time with scope cursors.
   - ✓ Screen capture of 100kHz 5 Vpp 2.5V dc square wave input and output voltage for $Z_L = \infty$ and diode from base to collector. Measurement of rise time, fall time, and storage time with scope cursors.

3. Standard TTL Inverter
   - ✓ Screen capture of output voltage versus input voltage for $Z_L = \infty$. Adjust x & y scales so that plot uses most of the scope screen.
   - ✓ Measurement of VIL, VIH, VOL, VOH, NML, and NMH with scope cursors. Reference Fig. 8.7 and Eqns. 8.1 & 8.2.
   - ✓ Screen capture of 100kHz 5 Vpp 2.5V dc square wave input and output voltage for $Z_L = \infty$.
   - ✓ Screen capture of 100kHz 5 Vpp 2.5V dc square wave input and voltage at collector of Q3.
   - ✓ Previous two requirements repeated for f changed to 1MHz.

4. 74LS TTL Inverter
   - ✓ Screen capture of output voltage versus input voltage for $Z_L = \infty$. Adjust x & y scales so that plot uses most of the scope screen.
   - ✓ Measurement of VIL, VIH, VOL, VOH, NML, and NMH with scope cursors. Reference Fig. 8.7 and Eqns. 8.1 & 8.2.
   - ✓ Screen capture of 100kHz 5 Vpp 2.5V dc square wave input and output voltage for $Z_L = \infty$.
   - ✓ Screen capture of 1MHz 5 Vpp 2.5V dc square wave input and output voltage for $Z_L = \infty$.
   - ✓ Measurement of average power dissipation per gate for no input, 100kHz 5 Vpp 2.5V dc square wave input, and 1MHz 5 Vpp 2.5V dc square wave input.
   - ✓ Measurement of ring oscillator frequency and calculation of propagation delay t_p. Measurement of power dissipation P_D of ring oscillator. Calculation of t_pP_D.

5. CMOS Inverter
   - ✓ Screen capture of output voltage versus input voltage for $Z_L = \infty$. Adjust x & y scales so that plot uses most of the scope screen.
   - ✓ Measurement of VIL, VIH, VOL, VOH, NML, and NMH with scope cursors. Reference Fig. 8.7 and Eqns. 8.1 & 8.2.
   - ✓ Screen capture of 100kHz 10 Vpp 5V dc square wave input and output voltage for $Z_L = \infty$.
   - ✓ Screen capture of 100kHz 10 Vpp 5V dc square wave input and output voltage for 1nF load cap.
   - ✓ Measurement of average power dissipation per gate for both a 100kHz 10 Vpp 5V dc square wave input and a 15MHz 10 Vpp 5V dc square wave input.
   - ✓ Measurement of ring oscillator frequency and calculation of propagation delay t_p. Measurement of power dissipation P_D of ring oscillator. Calculation of t_pP_D.