Georgia Institute of Technology

College of Engineering

School of Electrical and Computer Engineering

ECE 6416: Low-Noise Electronic Circuit Design

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Objective

The objective of this experiment is to design, simulate, evaluate experimentally and document a low-noise amplifier circuit. The equivalent input noise of the amplifier is to be minimized.

Target Design

Part 1: Circuit Topology

Figure 1 below shows the topology of the target circuit to be used for designing the low-noise amplifier. It consists of a common-emitter (CE) common-base (CB) cascode pair as the amplifier stage to provide voltage gain, followed by a DC-coupled common-collector (CC) low-impedance output stage. BJTs are intended to be used as the active devices.

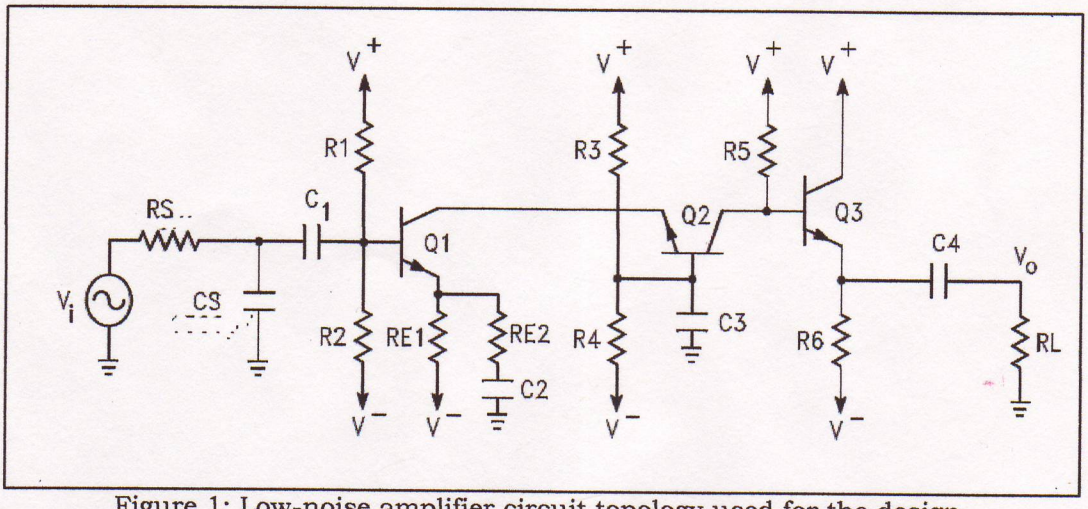

Figure 1: Low-noise amplifier circuit topology used for the design.

Part 2: Performance and Component Specifications

- DC Rail Power Supplies: ±15 V.
- Voltage Gain: 40 dB.
- Maximum Input Signal: 200 μV_{rms}.
- Lower Half-Power Cutoff Frequency: ≤ 20 Hz.
- Upper Half-Power Cutoff Frequency: ≥ 20 kHz.
- Total Harmonic Distortion (*THD*): ≤ 0.4 % at an output signal level of +10 dBm across a 600 Ω load resistor (according to standard audio signal level specifications) for an input sine wave with a frequency of 2 kHz. This is equivalent to a ~ 2.45 V_{rms} waveform across the load R_L.
- Source Impedance: R_S = 200 Ω.
- Shunt Capacitance at the input: C_S = 10 nF.

- Load Resistance R_L = 3 kΩ.
- Equivalent input noise voltage over the band 20 Hz to 20 kHz: ≤ 1 μV
- Active device choice: NPN BJT 2N3904 or 2N4401 measured during an earlier laboratory experiment must be used.
- Power supply decoupling network needs to be used for the rails.

Part 3: Simulation Specifications

The initial proposed design needs to be verified with SPICE circuit simulations. This simulation phase should precede the circuit assembly phase.

The default values for the BJT model parameters (IS, BF, RB, VA, CJC, CJE, TF) provided by the SPICE simulator should not be used. The values obtained from curve tracer measurements and manufacturer's datasheets must be used. The value of base spreading resistance (r_x) measured during an earlier experiment should be used as the SPICE model parameter RB.

A noise simulation of the circuit should be made to predict the signal-to-noise ratio (SNR) corresponding to an output signal level of +10 dBm into a load resistance of 600 Ω, as well as the noise figure of the amplifier.

The SPICE simulations should consist of the following parts:

- .OP (to verify the biasing or quiescent or the DC operating point of the circuit)
- .AC (to verify the frequency response and phase margin specifications)
- .TRAN (to examine the clipping and slew rate performance)
- .FOUR (to verify the THD specification)
- .NOISE (to verify the noise specifications)

Part 4: Measurement Specifications

The following parameters needs to be measured and reported for the designed circuit assembled on a breadboard.

- Mid-band Voltage Gain.
- -3 dB (or half power) bandwidth.
- Positive and Negative slew rates.
- THD at f = 2 kHz according to the conditions specified earlier.
- Quiescent operating point of the circuit.
- Output DC offset with input grounded.
- Equivalent input noise voltage.
- Signal-to-Noise-Ratio (SNR).
- Noise Figure: Spot Noise Figure at f = 2 kHz and the Total Noise Figure.

Design Philosophy

Gain and THD considerations

In the following description, transistor names refer to that on Figure 1, while voltages and currents with subscripts ending in 1, 2, and 3 refers to the transistor Q_1, Q_2, and Q_3 respectively.

The front stage of the amplifier is a cascode combination. In this configuration, Q_2 produces almost all of the voltage gain, while Q_1 provides some current gain and a low voltage gain (due to the low input impedance of the common-base stage Q_2), which reduces the high-frequency feedback through Miller effect. Q1 does raise the power level of the input signal to some extent. Given that the output stage (Q_3) is a common-collector configuration, it has a voltage gain close to unity. Therefore, Q_2 and its associated R_5 must be designed for voltage gain. Since we desire a very low THD, it is important that V_{CE2} is kept as large as possible, to allow for operation well within the linear region of Q_2. The same is true for Q_3. Note that while simply increasing R_5 is a tempting way to increase the gain, this also reduces V_{CE2}, which negatively affects the THD. To prevent this, if R_5 must be increased, I_{C1} must also be reduced. It is also desirable to operate Q_2 at a higher current level for an improved gain-bandwidth product.

R_{E2}, the negative feedback resistor at the emitter of Q_1, is critical in determining the overall gain of the circuit as well. As the gain of the Q_1 stage is low, it must be kept in mind that any small changes in it will be further multiplied by Q_2. This suggests that it is relatively easy to change the overall gain by simply tweaking R_{E2}. However, the gain provided by Q_1 must be kept low because V_{CE1} is relatively small, and an increased voltage swing can drive Q_1 into a highly non-linear region of operation, which worsens the THD. Therefore, even though no specific theoretical design for THD will be conducted, we will design for the best possible THD by biasing Q_2 and Q_3 in their linear region of operation, and Q_1 with a relatively low voltage gain, i.e., trying to keep R_{E2} relatively large for a feedback resistor (hundreds of ohms). Thus, keeping in mind THD considerations for the design, the base biasing network for Q2 is designed so that V_{CE2} is as large as possible (approximately 10 V). The reason this is possible is because by lowering V_{B2}, and assuming linear operation of Q_2, V_{E2} is also lowered, which increases V_{CE2}. The resistor used in this network will be small (tens of kilo-ohms) compared to those that bias Q1 (few mega-ohms) in order to make V_{B2} relatively insensitive to changes in I_{C2}.

Our choice of V_{CE2} being approximately 10V stems from the fact that V_{B3} must be approximately between 0V and 5V in order for Q_3 to operate in a linear region. This implies that V_{B1} is going to be between -10V and -15V (close to the

negative rail). However, we don't want to bias the base of Q1 too close to the negative rail because this calls for a small R_2, which worsens noise, as explained next.

Noise considerations

Clearly, the largest noise contribution happens at the input of the front stage. The base biasing network of Q_1 (formed by resistors R_1 and R_2) effectively presents a shunt resistance to the input of the amplifier. Therefore, it is important to use resistors as large as possible for this network (~ few mega-ohms or hundreds of kilo-ohms). The first step will be to determine the optimum-noise collector current for the cascode combination (I_C is approximately the same for both Q_1 and Q_2). Once this current is known, the base biasing network for the first stage is designed.

Another large contribution to the total noise is expected from the cascode combination of Q_1 and Q_2. One cannot simply state that Q_1 is the largest contributor to noise. Since the voltage gain of the Q_1 stage is low, the noise contribution of Q_2 can be significant too. Therefore, in finding the optimum-noise collector current for Q_1 and Q_2, we will analyze the cascode combination and not just Q_1 alone.

It is important to note that similar noise performance could be obtained with quite different frequency response of the amplifier. The topology used here is similar to using an overall feedback to get low-noise performance while simultaneously optimizing the gain-bandwidth product of the amplifier.

Device Parameter Measurements

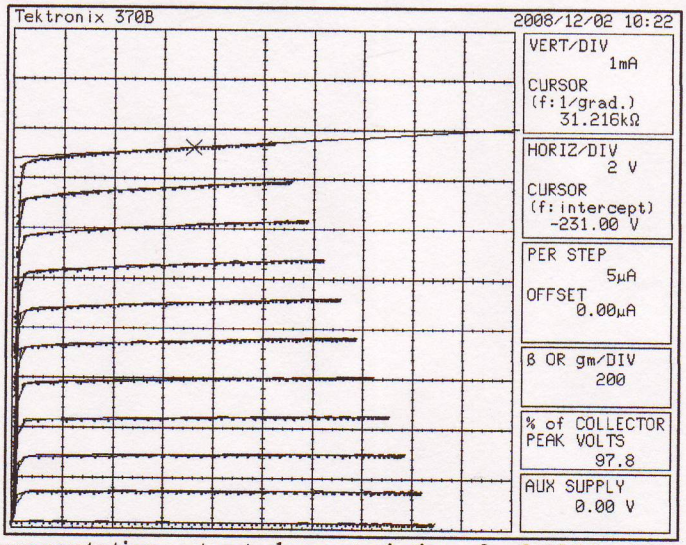

Figure 2: Representative output characteristics of a 2N3904 NPN BJT device.

The 2N3904 discrete NPN BJT device was chosen to be used for the low-noise amplifier design. Noise measurements were earlier performed on this device as a part of Lab 4 along with 2N4401, but the measurement results did not show much difference in noise performance between the two transistors. Most other parameters of interest are very close for these two transistors. 2N3904 was finally chosen as the device of interest for this design.

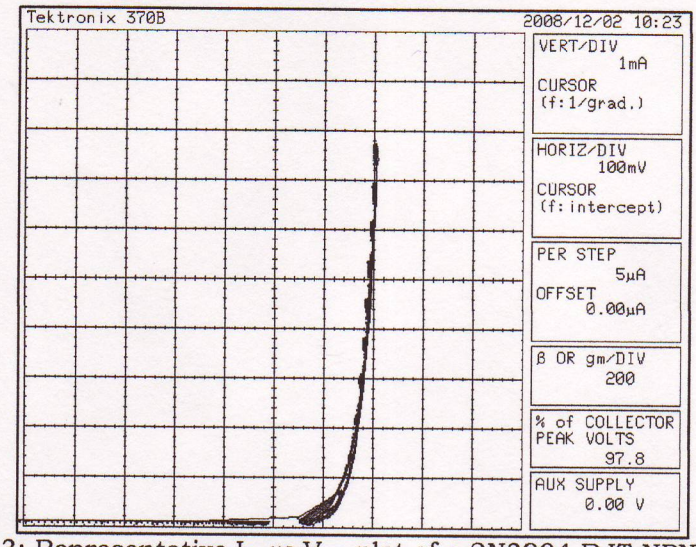

Figure 3: Representative I_C *vs* V_{BE} plot of a 2N3904 BJT NPN device.

Output characteristics of the 2N3904 devices (as in Figure 2) were used to calculate β, V_A, R_o for the transistors. From the previous laboratory experiment, the measured value of r_x was used. The rest of the relevant BJT SPICE model parameters were extracted from the manufacturer's datasheet. This modified BJT SPICE device model was used for the circuit simulations performed in the next part of the design procedure. This helps to make the models more realistic, which when used for designing circuits, would potentially give more reliable circuit simulation results.

Theoretical Calculations

Optimum-noise collector current for Q_1 and Q_2

A theoretical derivation for the optimum-noise collector current for the cascode combination was performed from equation 7.119 in the class notes, when flicker noise is neglected and it is assumed that $I_{C1} \approx I_{C2}$. Only the result is shown here:

$$I_{C(OPT)}^2 = \frac{\alpha\beta^2(\alpha\beta+1)V_T^2}{\alpha\beta^2(R_1+r_{x1}+R_2)^2+\alpha\beta[R_1+r_{x1}+(\beta+1)R_2]} \quad (1)$$

Where,

$\beta = \beta_1 = \beta_2$	:	common-emitter current gain for Q_1 and Q_2 (assumed equal)
$\alpha = \alpha_1 = \alpha_2$	:	common-base current gain for Q_1 and Q_2 (assumed equal)
r_{x1}	:	base spreading resistance of Q_1
R_1	:	(AC) source equivalent resistance
R_2	:	(AC) Q_1 external emitter equivalent resistance

For $\beta = 320$, $r_{x1} = 30\ \Omega$, $R_1 = 200\ \Omega$, $R_2 = 400\ \Omega$, the collector current that gives the optimum noise for the configuration is found to be $I_{C(OPT)} = 710\ \mu A$.

While Equation 1 above gives a good starting point for I_C, the fact that flicker noise was neglected will be found to be a weak assumption. A lower I_C will be used in an attempt to reduce flicker noise (which is directly proportional to I_C), and thus the total noise band power.

Small-signal voltage gain

A theoretical derivation for the overall small-signal voltage gain has been performed as well. In this derivation, the r_{out} (output impedance) of the BJTs was considered to be very large and thus neglected (based on measurements performed earlier during lab experiments). Also, the β (current-gain) for the transistors were considered to be large. Only the result is presented here:

$$A_v \approx \beta_1\beta_3 \frac{R_5}{R_5 + r_{\pi 3} + (\beta+1)r_{out}} \cdot \frac{r_{out}}{R_S + r_{\pi 1} + (\beta_1+1)r_{e,1}} \approx \left[\frac{R_5}{r_{e,1} + \frac{R_S + r_{\pi 1}}{\beta_1}} \right] \left[\frac{r_{out}}{r_{out} + \frac{R_5 + r_{\pi 3}}{\beta_3}} \right] \quad (2)$$

Where,

r_{out}	:	$R_6 // R_L$, the equivalent load resistance at the output
r_{e1}	:	$R_{E1} // R_{E2}$

As expected, R_5 and r_{e1} (the equivalent emitter AC resistance of Q_1) play an important role in determining the gain. The design procedure will first fix r_{out} based on Q_3 biasing considerations, which will then leave R_5 and R_{E2} as the most important contributors to the voltage gain. A constant ratio between R_5 and R_{E1} will keep the bias voltages approximately constant for Q_1 and Q_2.

Theoretical calculations for component values

A first set of values for the passive components based on the following rationale were computed and is shown below:

- All capacitors large enough to obtain a low lower cut-off frequency: **47 µF**.
- $\beta = 320$ for all BJTs.
- For low noise: $I_{C1} = I_{C(OPT)} = 710\ \mu A$. Thus, $I_{B1} = 2.21\ \mu A$.

- For large voltage swing at the output: I_{C3} = 2 mA, V_{E3} = 0 V. Thus, **R_6 = 7.5 kΩ**.
- $r_{out} = R_6 // R_L$ = 2.14 kΩ.
- $r_{\pi 1} = \beta_1 V_T / I_{C1}$ = 11.3 kΩ.
- $r_{\pi 3} = \beta_3 V_T / I_{C3}$ = 4.0 kΩ.
- Choose R_1 as a very large resistor: **R_1 = 3 MΩ**.
- Select V_{B1} to be between -10 V and -15 V, not too close to -15 V: V_{B1}= -11 V.
- Thus, R_2 can be computed: **R_2 = 620 kΩ**.
- **R_{E1}** = $(V_{B1} - V_{BE1})/I_{E1}$ = **4.7 kΩ**.
- Total current through R_5: $I_{R5} = I_{C(OPT)} + (I_{C3}/\beta_3)$ = 716 μA.
- Therefore, **R_5** = (+15 V - 0.7 V)/ I_{R5} = **20 kΩ**.
- To achieve A_v = 100, from equation 2, r_{e1} = 157 Ω. Thus, **R_{E2} = 162 Ω**.
- R_3 and R_4 are chosen somewhat arbitrarily to ensure that V_{B2} = -5 V. Make the sum of its resistances no more than 40 kΩ (see the THD considerations section). Thus, **R_3 = 27 kΩ** and **R_3 = 13 kΩ**.

The next phase in the design procedure is to simulate the circuit with the component values calculated theoretically above.

Circuit Simulation Results

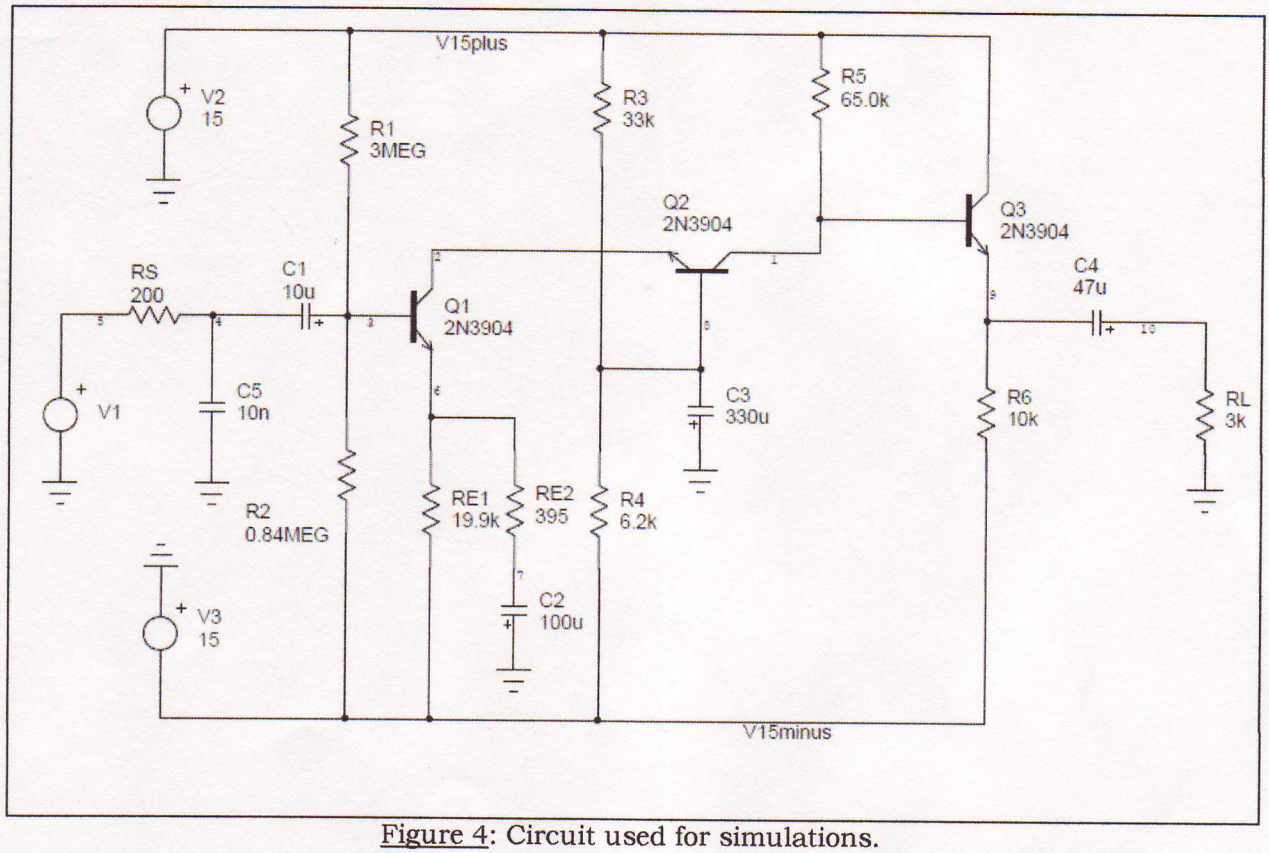

Figure 4: Circuit used for simulations.

- Multiple SPICE based circuit simulation software packages were tried like LTSpice, Agilent ADS, etc. Finally, Intusoft SPICE was used as the circuit simulation software of choice to optimize convenience with access, installation and capabilities of the package.
- A snapshot of the circuit schematic used for the simulations is shown in Figure 4.
- The following simulation deck shows the BJT model used:

```
.AC DEC 1001 1 1MEG
.OP
.TRAN 0.005M 5M 0 0.005M
.NOISE V(10) V1 DEC 1001 20 20K  1
.PRINT NOISE INOISE ONOISE
.FOUR 2000 V(10)
.OPTIONS ACCT
Q1 2 3 6 _Q1_MOD
.MODEL _Q1_MOD NPN AF=1.0 BF=320 BR=7.5 CJC=3.5PF CJE=4.5PF
+ IKF=.025 IS=1.4E-14 ISE=3E-13 KF=9E-16 NE=1.5 RB=30 RC=2.4
+ TF=4E-10 TR=21E-9 VAF=231 XTB=1.5
Q2 1 8 2 _Q2_MOD
```

```
.MODEL _Q2_MOD NPN AF=1.0 BF=320 BR=7.5 CJC=3.5PF CJE=4.5PF
+ IKF=.025 IS=1.4E-14 ISE=3E-13 KF=9E-16 NE=1.5 RB=30 RC=2.4
+ TF=4E-10 TR=21E-9 VAF=93.92 XTB=1.5
Q3 V15PLUS 1 9 _Q3_MOD
.MODEL _Q3_MOD NPN AF=1.0 BF=320 BR=7.5 CJC=3.5PF CJE=4.5PF
+ IKF=.025 IS=1.4E-14 ISE=3E-13 KF=9E-16 NE=1.5 RB=30 RC=2.4
+ TF=4E-10 TR=21E-9 VAF=116.72 XTB=1.5
R1 V15PLUS 3 3MEG
R2 3 V15MINUS 0.84MEG
C5 4 0 10N
RS 5 4 200
V1 5 0 DC=0 AC=1 SIN 0 35.4M 2K 0
RE1 6 V15MINUS 19.9K
RE2 6 7 395
R5 V15PLUS 1 65.0K
C2 0 7 100U
R3 V15PLUS 8 33K
R4 8 V15MINUS 6.2K
C3 0 8 330U
R6 9 V15MINUS 10K
C4 10 9 47U
RL 10 0 3K
C1 3 4 10U
V2 V15PLUS 0 DC=15 AC=0
V3 0 V15MINUS DC=15 AC=0
.END

.END
```

Circuit Simulation Tradeoffs

The following tradeoffs were encountered while designing the circuit for the specified performance levels:

- Increasing gain by simply lowering R_{E2} worsens (increases in percentage) THD.
- Increasing gain with R_5 worsens THD.
- Increasing gain by lowering R_{E1} changes THD. There was an optimum value for R_{E1}, around 19.9kΩ. This is due to a change in the bias point of Q_1 as a result of changing R_{E1}.
- Simultaneously changing R_{E2} and R_5 helped in minimizing THD.
- Increasing the current in Q_3 by reducing R_6 helps in minimizing the THD at the output to some extent. Again, there was an optimum value for R_6.
- Reducing V_{B1} by reducing R_2 helps in getting a much higher voltage swing at the output but increases the noise if the value is small enough.
- I_{C1} and I_{C2} can be increased by reducing R_5 and R_{E1}, but their ratios should be constant to keep V_{CE1} and V_{CE2} at a fixed level.
- Tweaking some of the capacitors can change THD, but only to a very small level.

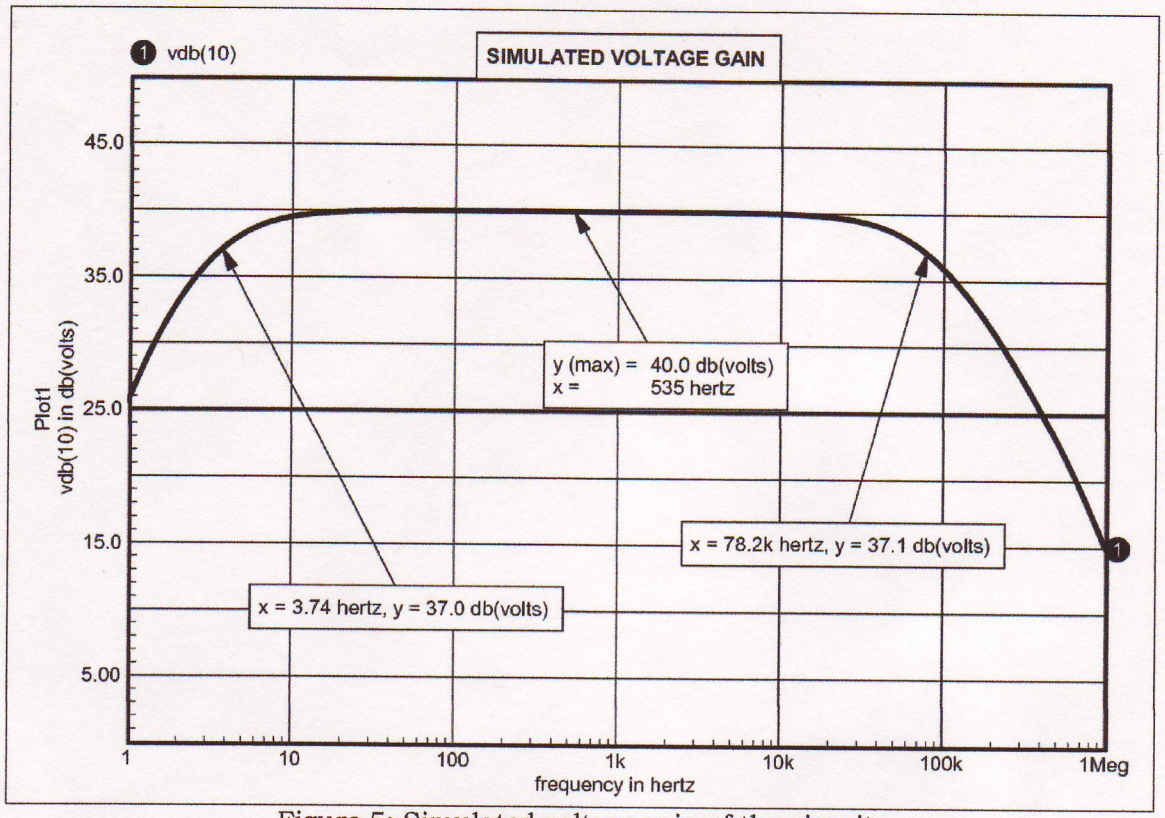

Figure 5: Simulated voltage gain of the circuit.

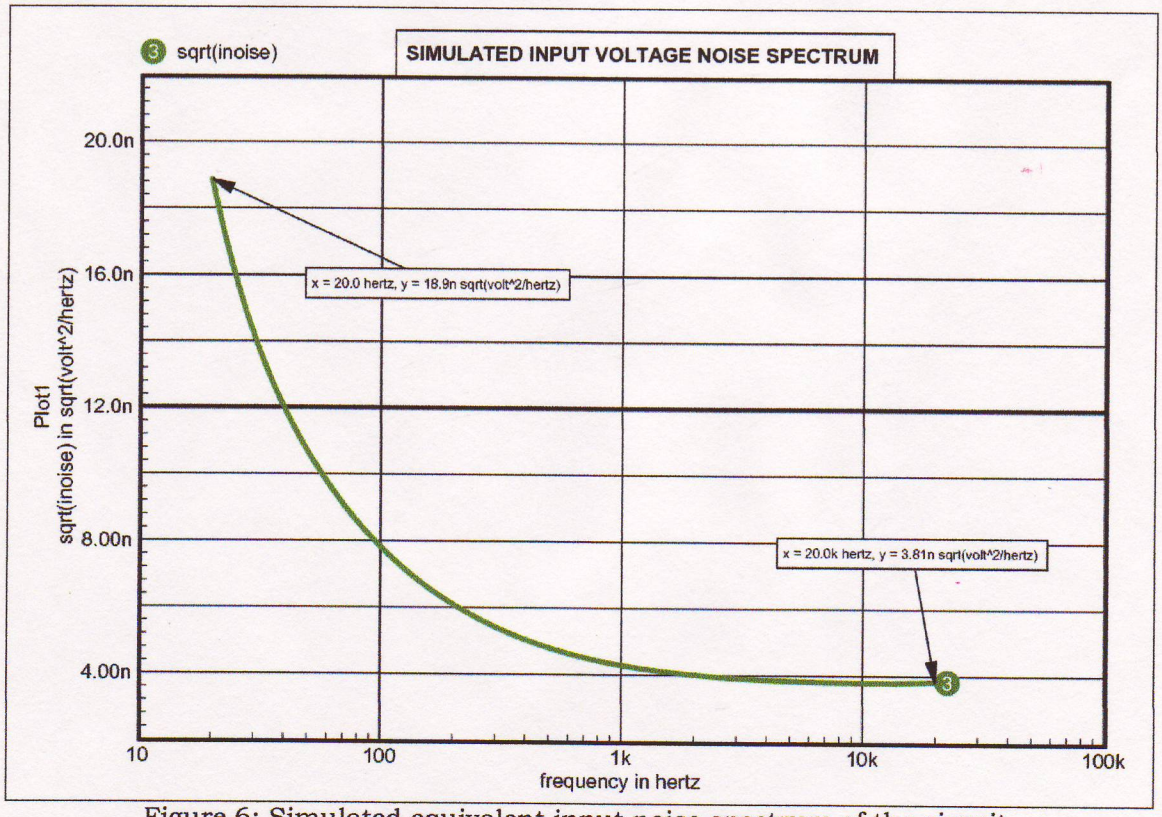

Figure 6: Simulated equivalent input noise spectrum of the circuit.

Experimental Results

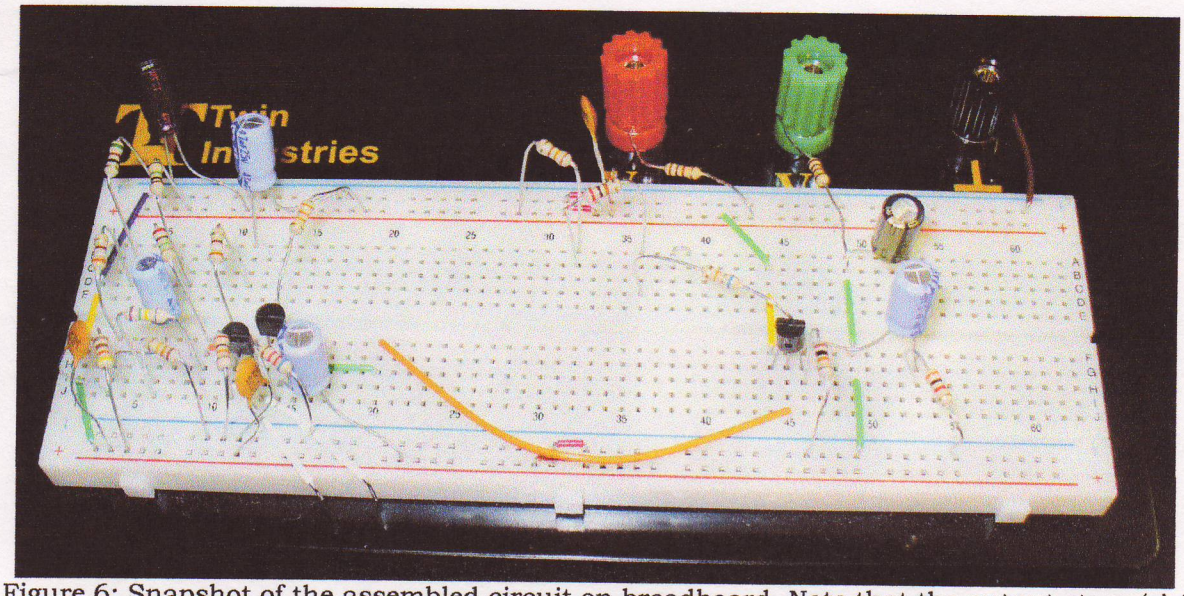

Figure 6: Snapshot of the assembled circuit on breadboard. Note that the output stage (right) was placed away from the cascode combination (left) to prevent positive feedback that could lead to oscillations.

Frequency Response Measurement

- The HP 33120A Function Generator (a 24.5 mV_{rms} sine wave output with 2 kHz frequency and 50 Ω output resistance) was used for measuring the gain and bandwidth of the amplifier. The output waveforms were measured on the Tektronix 754D Digital Oscilloscope. The frequency of the input signal was varied over a wide range to calculate the gain of the op-amp stage alone. The measured input voltage V_i at 2 kHz = 24.59 mV_{rms}.
- The measured output voltage V_o at 2 kHz (mid-band) = 2.493 V_{rms}.
- The -3dB frequencies were measured as f_L = 17.8 Hz and f_H = 77 kHz.
- The -3dB (or half-power) frequencies were identified as frequency points where the output voltage was $1/\sqrt{2}$ times the mid-band output voltage. For this the frequency was varied continuously using the function generator.
- The measured gain = 101, which is > 40 dB and satisfy the design specification for the amplifier.

Total Harmonic Distortion Measurement

In order to measure THD, a 2 kHz sinusoidal input signal is fed to the amplifier such that the output is a waveform with 2.45 V_{rms} (+10 dBm for a 600 ohm resistor audio standard). The THD of this output signal is then measured with the DSA. The input and the output signal during the THD measurement

are shown in Figures 7 and 8. The spectrum of the output signal including the fundamental and harmonic frequencies is shown in Figure 9.

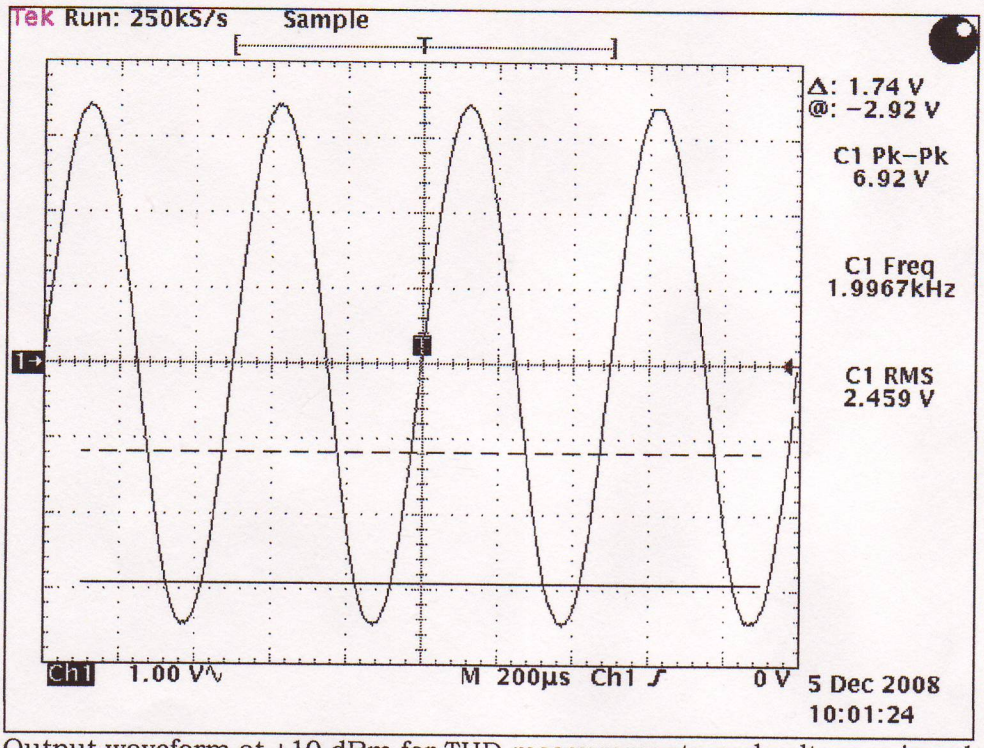

Figure 7: Output waveform at +10 dBm for THD measurements and voltage gain calculations.

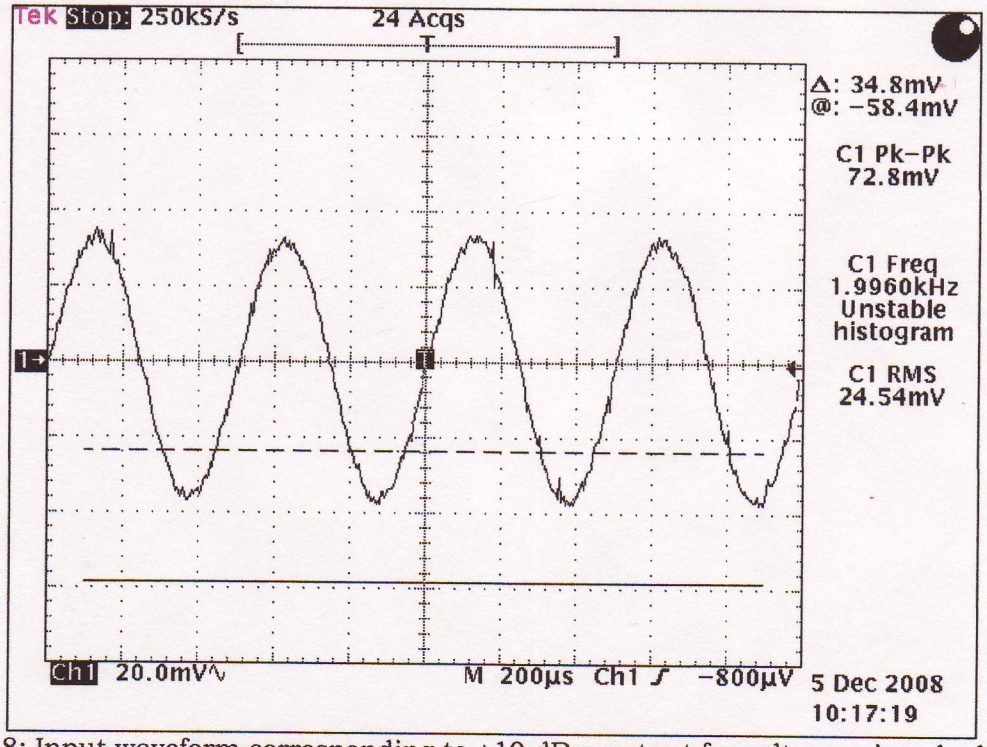

Figure 8: Input waveform corresponding to +10 dBm output for voltage gain calculations.

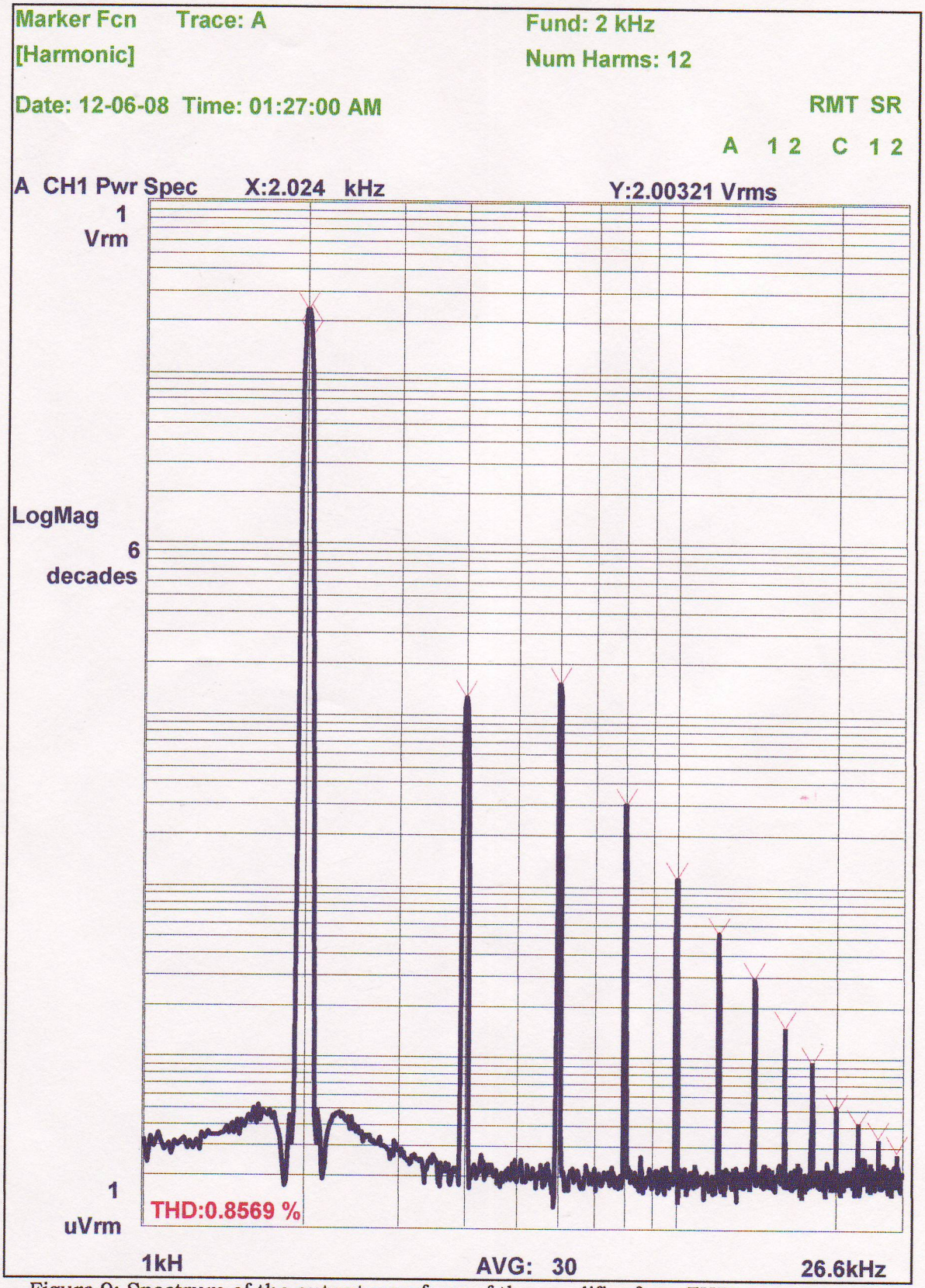

Figure 9: Spectrum of the output waveform of the amplifier from THD measurement.

A high peak for the third-harmonic in Figure 9 indicates that the output voltage swing is asymmetric, which was proved right as the negative swing was clipped before the positive swing when the output signal level was increased (beyond specifications, just for verification purposes).

Noise Measurement

The component values used for the simulation deck led to a much higher noise level experimentally than predicted by simulation results. The reason was attributed to a high flicker noise component at the theoretical optimum I_c for Q_1 and Q_2. This led to the decision of using a lower than optimum I_C for biasing Q_1 and Q_2. It was experimentally determined that $I_C \sim 200\ \mu A$ brought the total input noise down, and therefore, this collector current level was chosen. Additionally, in order to lower flicker noise further down, the lower cut-off frequency was raised from 3 Hz to 17 Hz. This was achieved by reducing C_1 from 47 μF to 1 μF. The total and spot noise were measured when the input was shorted ($R_S = 200\ \Omega$). The SNR and noise figure were computed as follows:

$$SNR = 10\log\left(\frac{v_{so}^2}{v_{no}^2}\right)$$

$$NF = 10\log\left(\frac{\frac{v_{ni}^2}{\Delta f}}{4kT_oR_S}\right) \qquad (3)$$

Where,

v_{so}	:	amplitude of the output waveform
v_{no}	:	total output noise voltage
v_{ni}	:	total input noise voltage

All of these helped in reducing the equivalent output noise voltage, which was measured using the DSA. The final measured equivalent output noise voltage is shown in Figure 10 below. When this value is divided by the voltage gain A_v, it gives the equivalent input noise voltage. From the measured value in Figure 10, the equivalent input noise voltage is < 1 μV, which satisfies the target design specification for the amplifier. The bandwidth used for measurement of the spot noise voltage by the DSA is 61.11 Hz.

The SNR, the Noise Figure at 2 kHz and the Total Noise Figure for the amplifier are calculated using the measurement data in Figure 10 (total band 20Hz to 20kHz noise RMS-voltage, or v_{no}) and are provided in Table 1 below. All noise measurements were done when the input was grounded. To get a pessimistic noise measurement, we substituted the function generator with a 50Ω resistor to ground, in addition to the 150Ω resistor already in place.

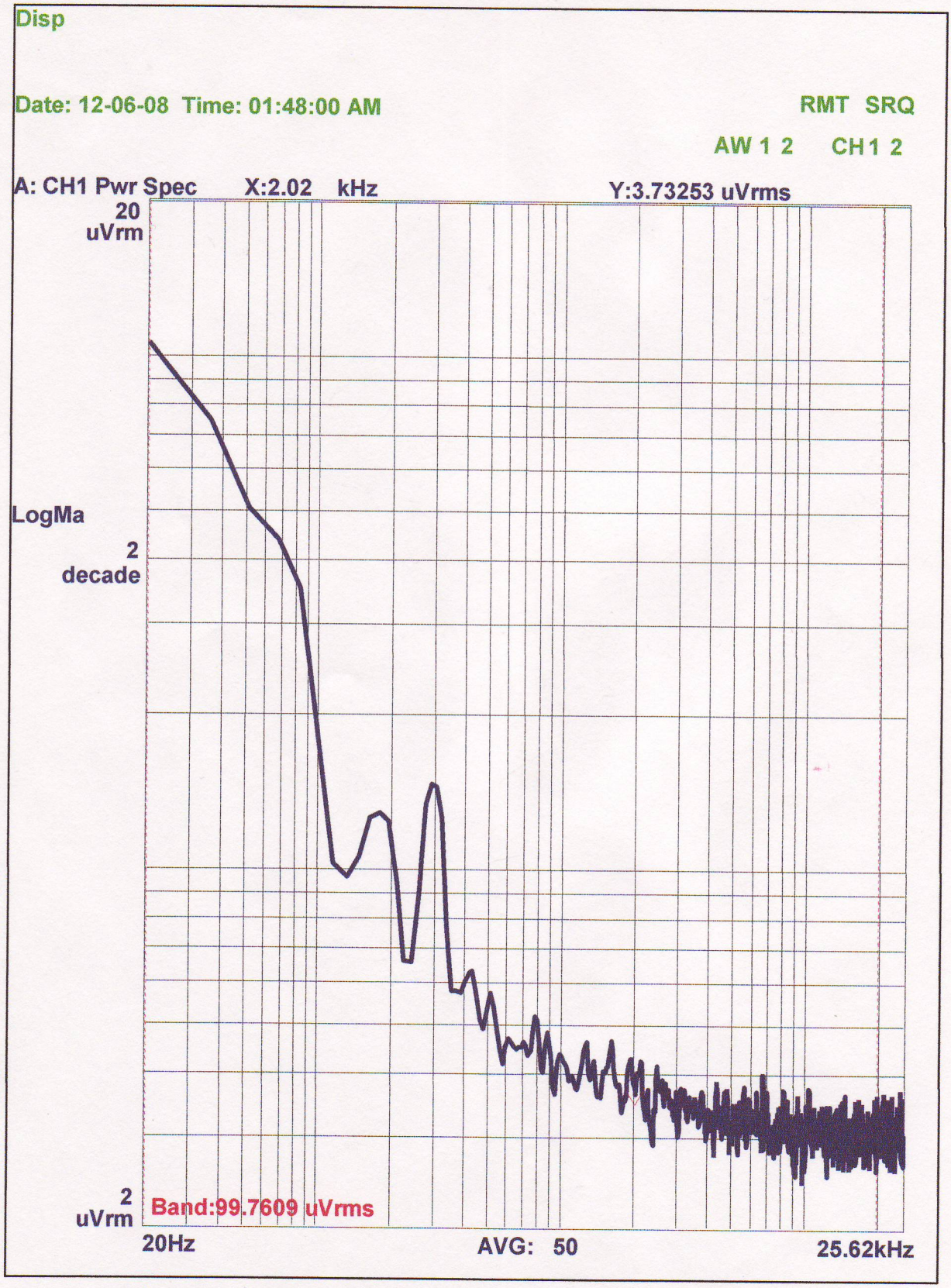

Figure 10: Noise Spectrum measured at the output of the amplifier.

Slew-Rate Measurement

Slew rate measurements were performed by feeding the amplifier with a 25 mV_{rms} square wave at 2 kHz frequency (high enough to see the slope in the output waveform corresponding to the edges of the input square waveform). The maximum slope of the rising and falling edges of the output waveform were measured and recorded as positive and negative slew rates respectively. Figures 11 and 12 show the rising and falling edges of the output waveform respectively along with the slew rate measurement setup. The positive and negative slew rates measured were 1.44 V/μs and 1.4 V/μs respectively.

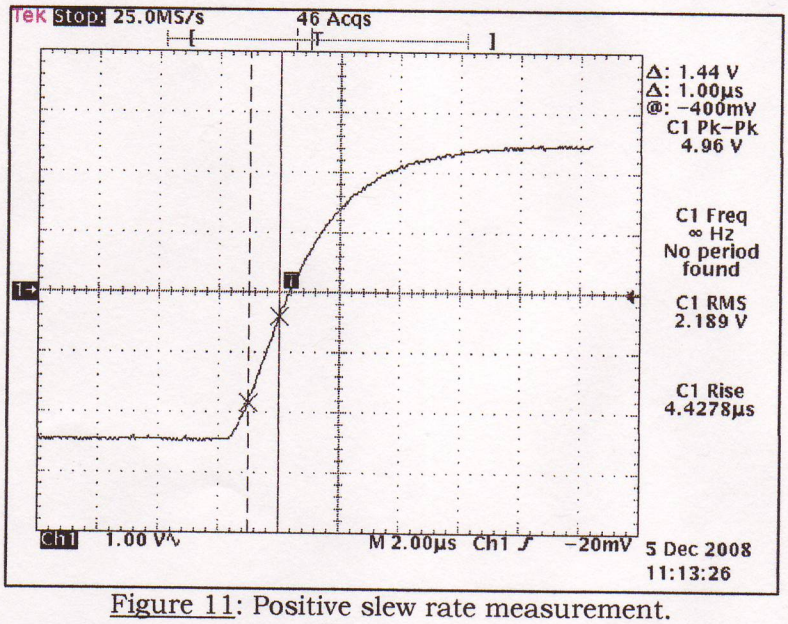

Figure 11: Positive slew rate measurement.

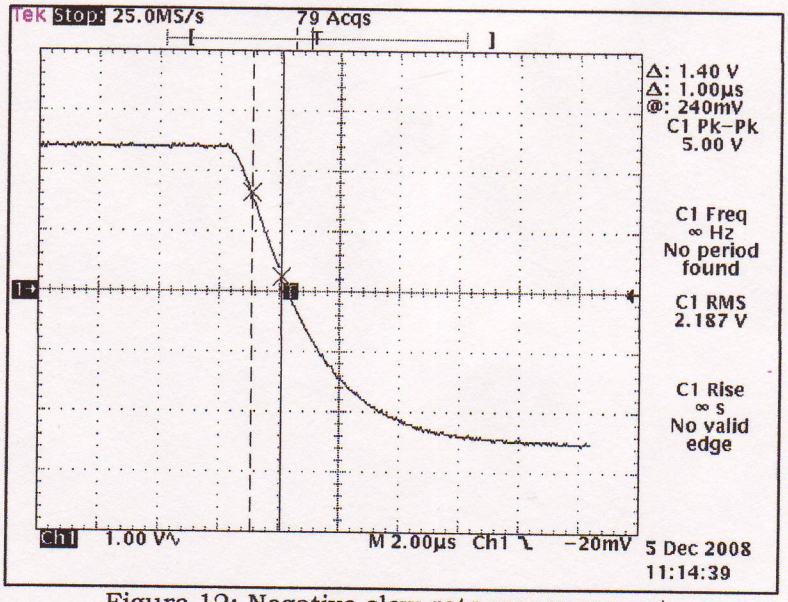

Figure 12: Negative slew rate measurement.

Experimental Tradeoffs

Most of the tradeoffs encountered while assembling and testing the designed circuit on a breadboard includes the issues which were assessed theoretically and/or by simulations and has been discussed earlier in this report.

The various tradeoffs taken care of during the noise measurements were the most dominant ones. In each case, either or both gain and THD were the tradeoffs to minimize noise. In an extreme case, changing capacitors to affect the noise and THD could adversely affect the frequency response of the amplifier.

Deviations of the experimental design and results from the simulated version could be attributed to the deviation of actual device parameter values from those used in simulations. Temperature should also be kept in mind, as the lab where the measurements were taken was, at times, considerably warmer than T_o). We found that the DC circuit performance was very sensitive to the (ratio) of values of R_1 and R_2, as these components play a big role in fixing V_{B1}. The circuit AC performance is sensitive to some of the component values (in particular R_5 and R_{E2}), and since the component values are different from their nominal values due to tolerance in their values, some of these experimental variations (compared to simulation) can be attributed to the distribution of component values.

Table 1: Simulated and realized circuit performance and components.

Parameter	**Simulated**	**Realized or measured (nominal)** *(final values, after circuit modifications)*
A_v (Voltage Gain)	40.0 dB	40.1 dB
f_L (lower -3dB frequency)	3.74 Hz	17.8 Hz
f_H (upper -3dB frequency)	74.2 kHz	77.0 kHz
Output Offset Voltage	0 V	50 µV
Max. output voltage swing	7.25 V_{pp}	7 V_{pp}
Max.input voltage swing	74.9 mV_{pp}	71.1 mV_{pp}
THD	0.95 %	0.86 %
v_{ni}	0.558 μV_{rms}	0.988 μV_{rms}
Positive Slew Rate	1.52 V/µs	1.44 V/µs
Negative Slew Rate	1.50 V/µs	1.40 V/µs
SNR	92.5 dB	87.8 dB
NF @ 2 kHz	6.99 dB	8.44 dB
Total NF	6.86 dB	11.8 dB
V_{B1}	-10.4 V	-10.46 V
V_{CE1}	0.10 V	0.15 V
V_{CE2}	12.34 V	11.34 V
V_{CE3}	14.22	14.64 V
I_{C1}	202 µA	200 µA
I_{C2}	204 µA	205 µA
I_{C3}	1.58 mA	1.57 mA
R_1	3.0 MΩ	3.007 MΩ (3 MΩ)
R_2	0.84 MΩ	894.1 kΩ (880 kΩ)*
R_{E1}	19.9 kΩ	19.73 kΩ (20 kΩ)
R_{E2}	395.0 kΩ	389.1 Ω (390 Ω)
R_3	33.0 kΩ	32.77 kΩ (33 kΩ)
R_4	6.2 kΩ	6.11 kΩ (6.2 kΩ)
R_5	65.0 kΩ	67.58 kΩ (68.33 kΩ)*
R_6	10.0 kΩ	9.79 kΩ (10 kΩ)
R_L	3.0 kΩ	2.956 kΩ (3 kΩ)
C_1	10 µF	1 µF
C_2	100 µF	47 µF
C_3	330 µF	47 µF
C_4	47 µF	47 µF

*Notes:

- R_2 achieved as a series combination of 750kΩ and 130kΩ.
- R_5 achieved as a series combination of 68kΩ, 200Ω and 130Ω.

Discussion of Results

The experimental and simulation results are tabulated in Table 1 above for comparison. The following comments can be made about the results:

- The simulation results and experimental results compare very well for the DC bias currents and voltages for the devices.
- The passive component values used for design of the circuit compares closely between simulation and experiment.
- The gain and frequency response of the circuit compares very well between simulation and experiment.
- The experimentally measured noise value is much higher compared to that from simulations, as the setup is not designed to avoid any external interference from other stray noise sources, nor temperature higher than T_o.
- The measured equivalent input noise voltage meets the specification given for the circuit.
- The measured THD is low, but it does not meet the design specification. This is mainly because of Q_1 which might have been pushed to the edge of the linear region while tweaking around with experimental component values. It was decided to meet the gain, frequency response, and -most importantly- noise specifications while still achieving a THD <1% for the amplifier.
- The THD can be improved to the specified level by reducing R_5, but gain would be traded-off during the process, even after compensating with R_{E2}.

Conclusions

All the design specifications for the low-noise amplifier were met by the design except the THD specification. The main reason for this was because of the input stage moving close to the edge of the linear region almost into saturation. This circuit could be further optimized to reduce the THD and meet all the specifications with further time and effort. Still, THD=0.86% was better than the 0.95% predicted by SPICE, due to minor adjustments to the bias point of Q_1 that were done "in the field".

The measurement technique could be improved by using a much larger breadboard to minimize the noise from capacitive coupling. Additionally, it would definitely help to use a shielded metallic box for the noise measurements. Further improvements could result from using better SPICE device models for circuit simulation of the low-noise amplifier.

It was also verified in this circuit that the theoretical optimum collector current obtained when flicker noise is neglected is not accurate. If low frequencies of operation are of interest -as is the case here- then the collector

current for the front cascade stage should be chosen as small as possible. Another flicker noise-reduction technique that gave good results was to raise the lower cut-off frequency of the amplifier, so that more lower-frequency flicker noise gets "cut-off". One must keep in mind that at the frequencies of tens of Hz, the flicker noise is by far the larger contributor to the total noise.